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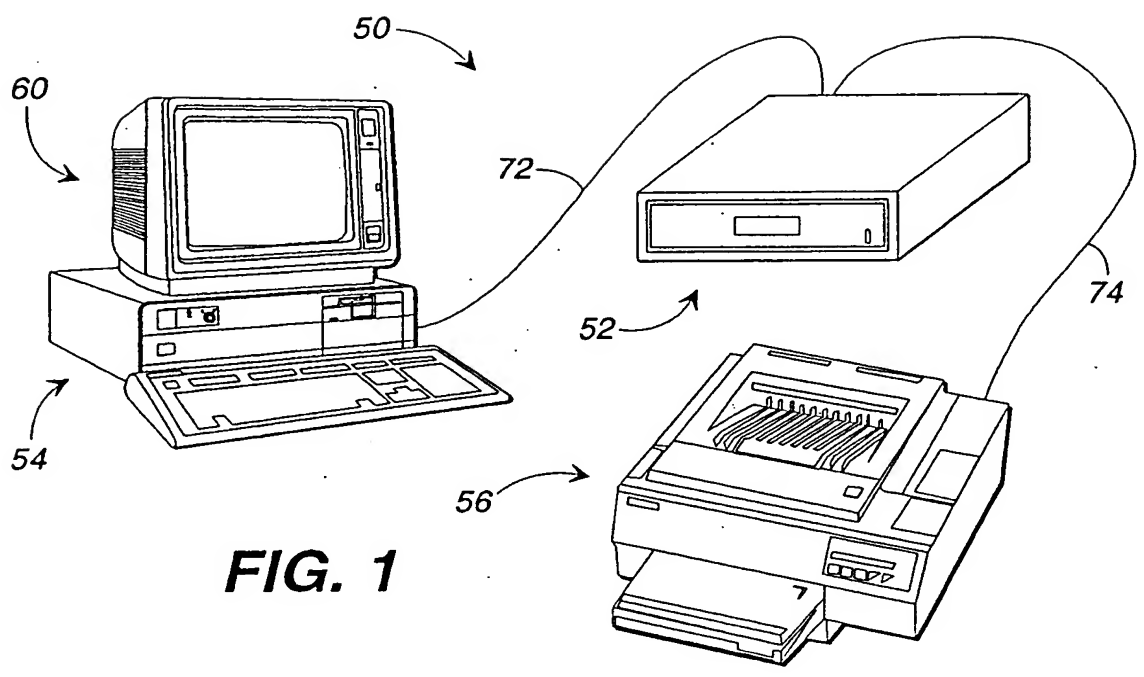


FIG. 1

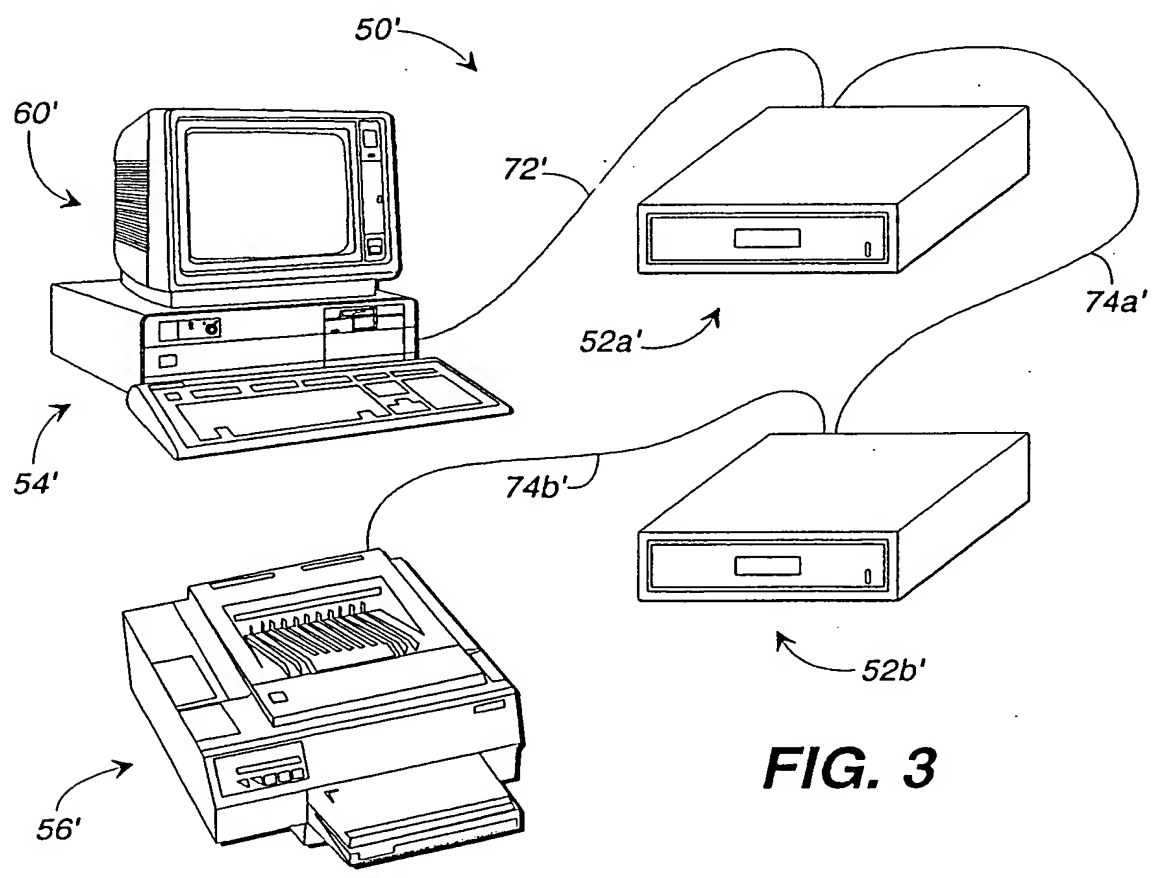
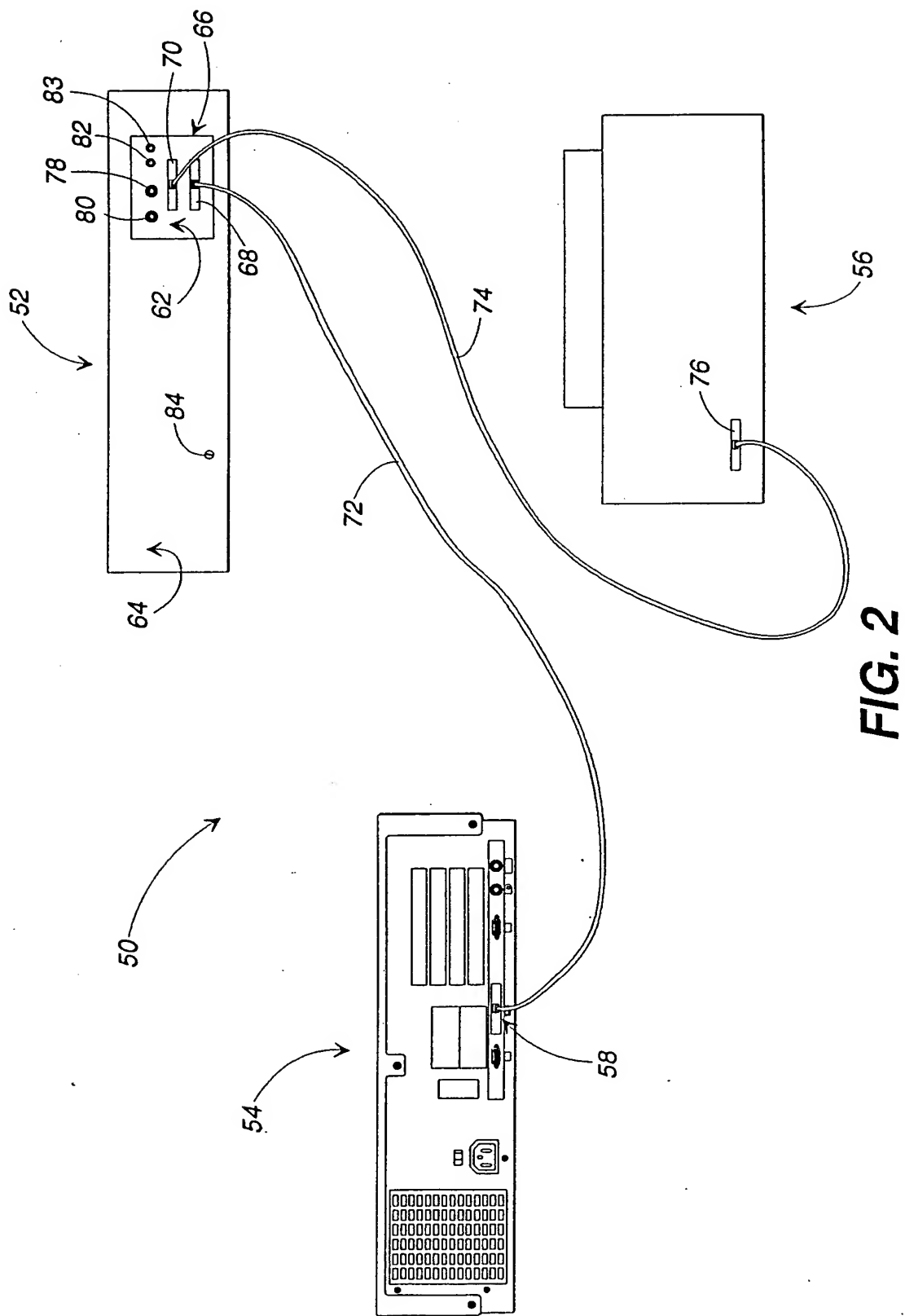


FIG. 3



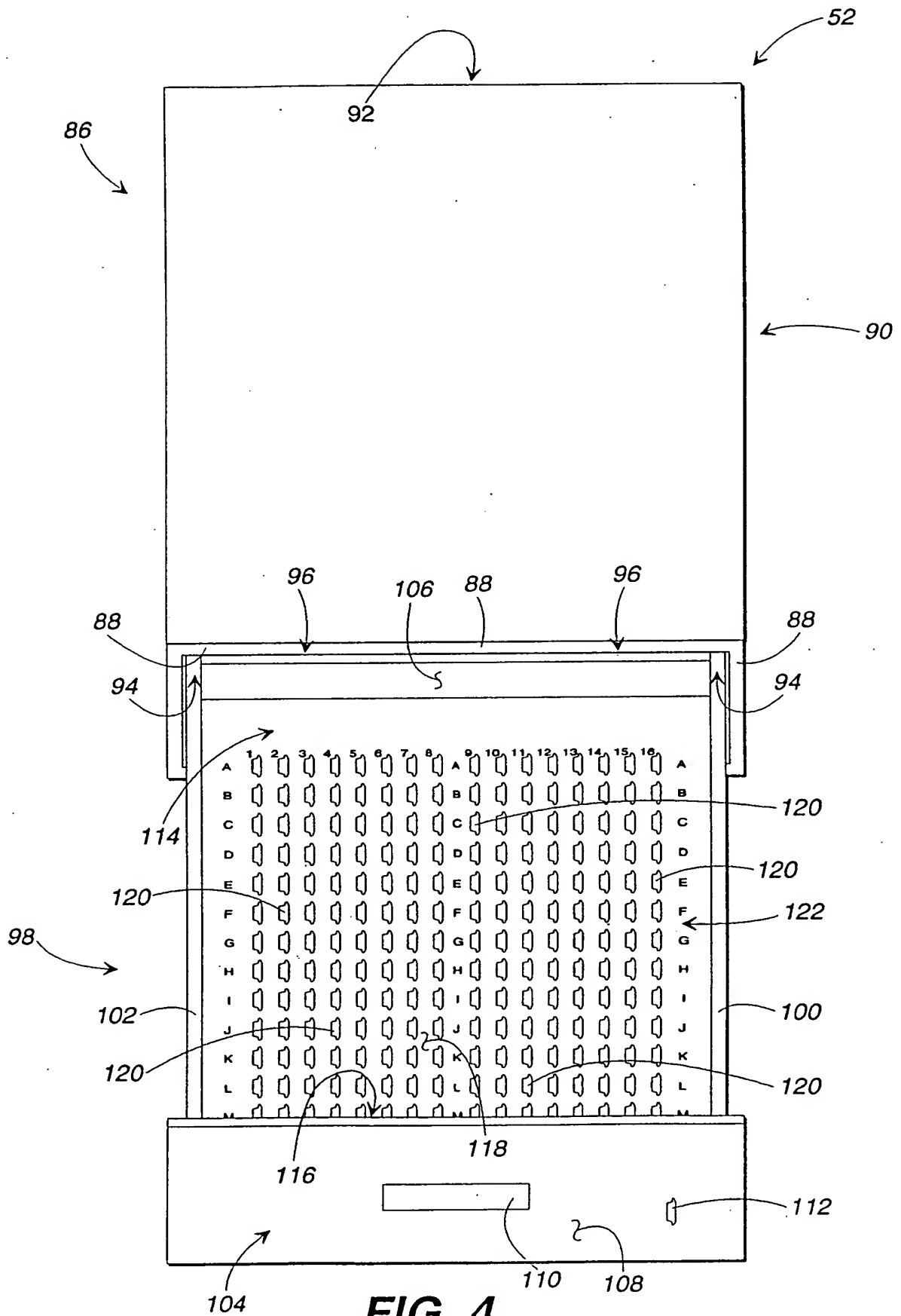


FIG. 4

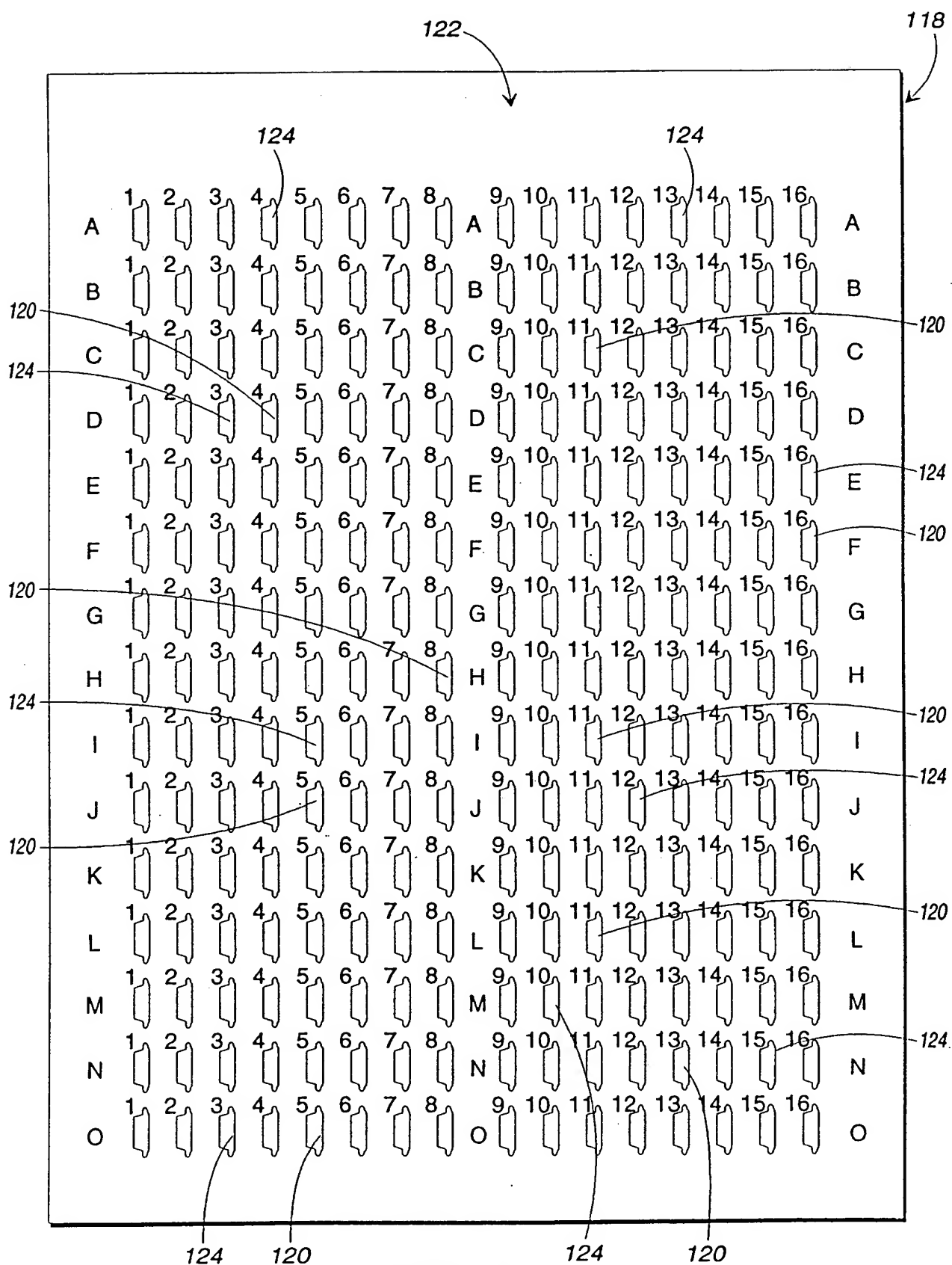


FIG. 5

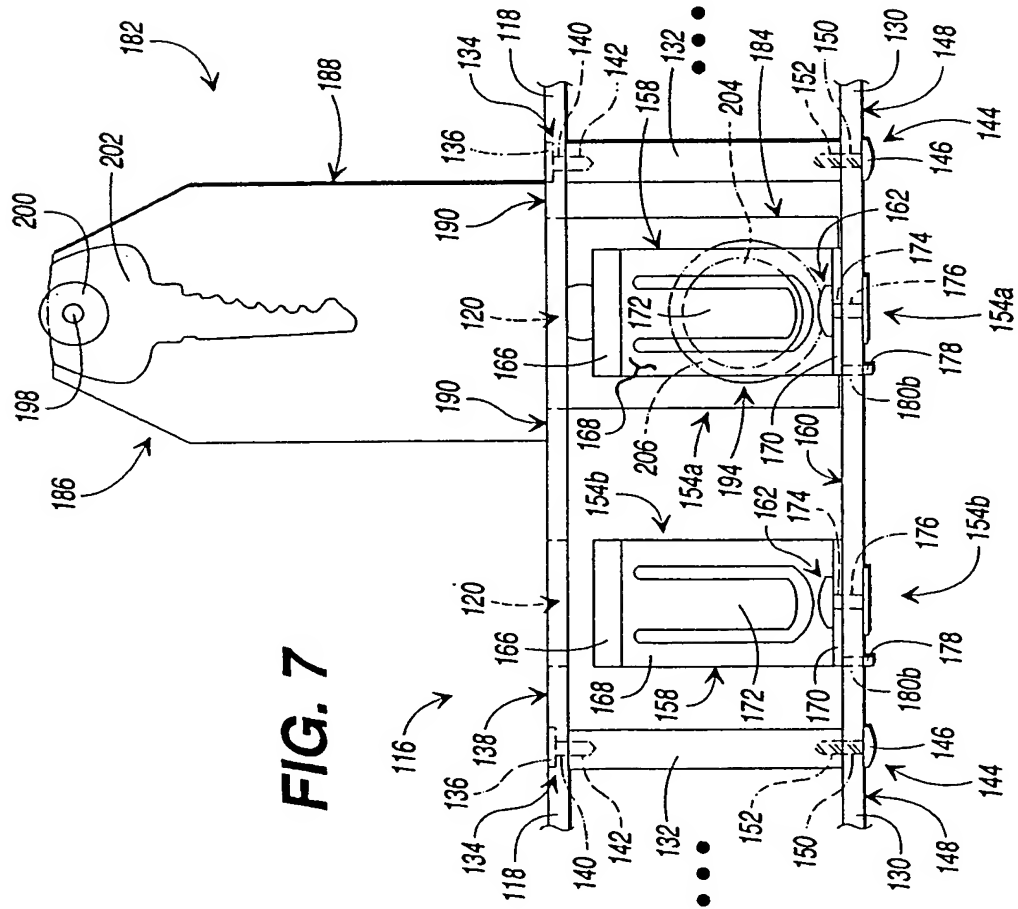


FIG. 7

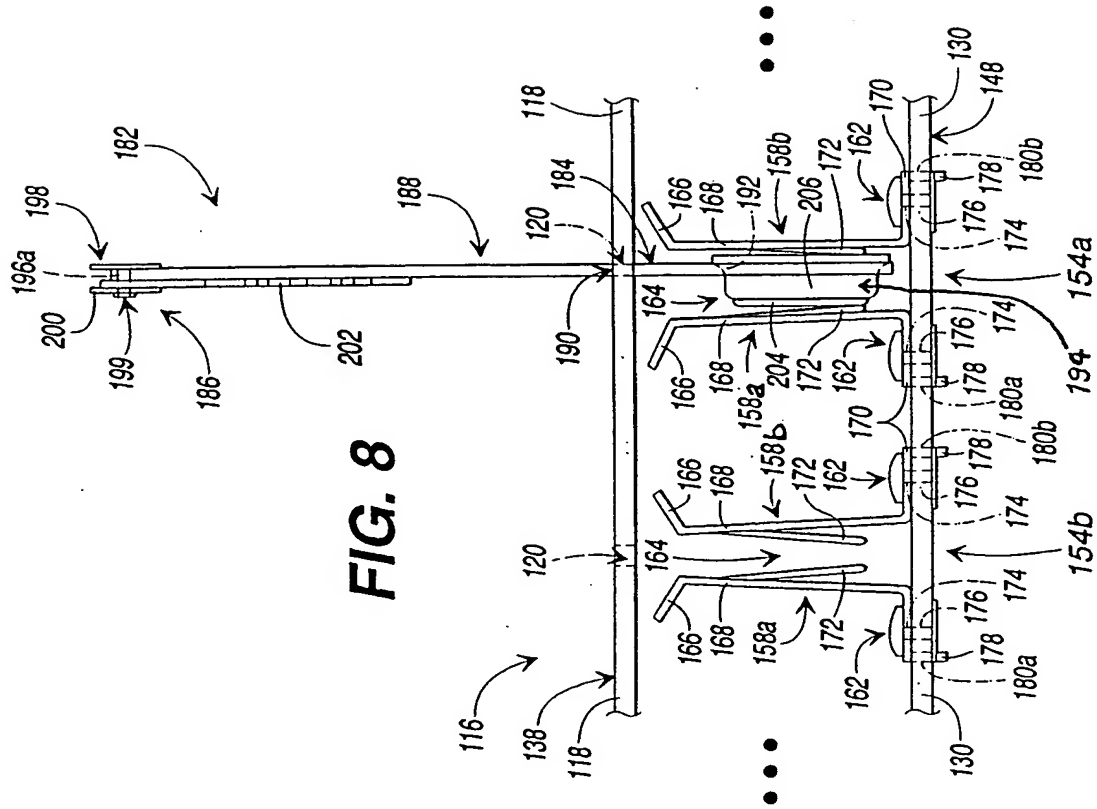


FIG. 8

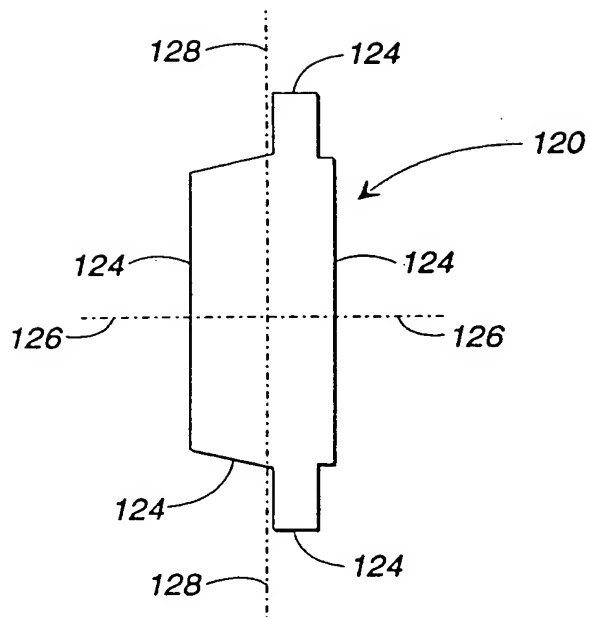


FIG. 6

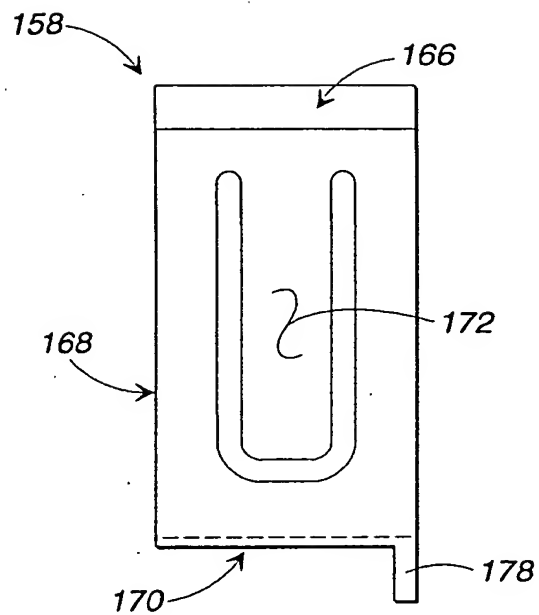


FIG. 9

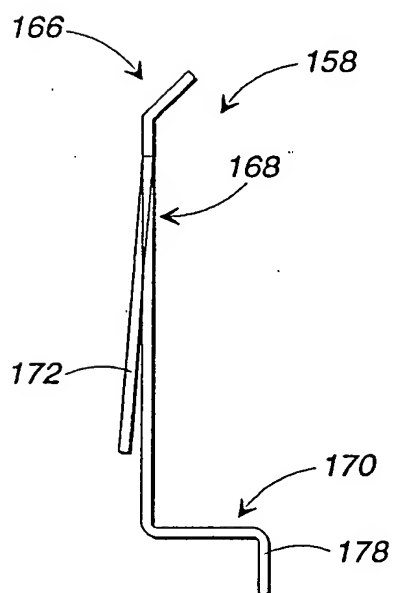


FIG. 10

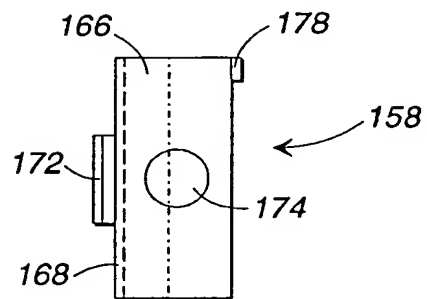


FIG. 11

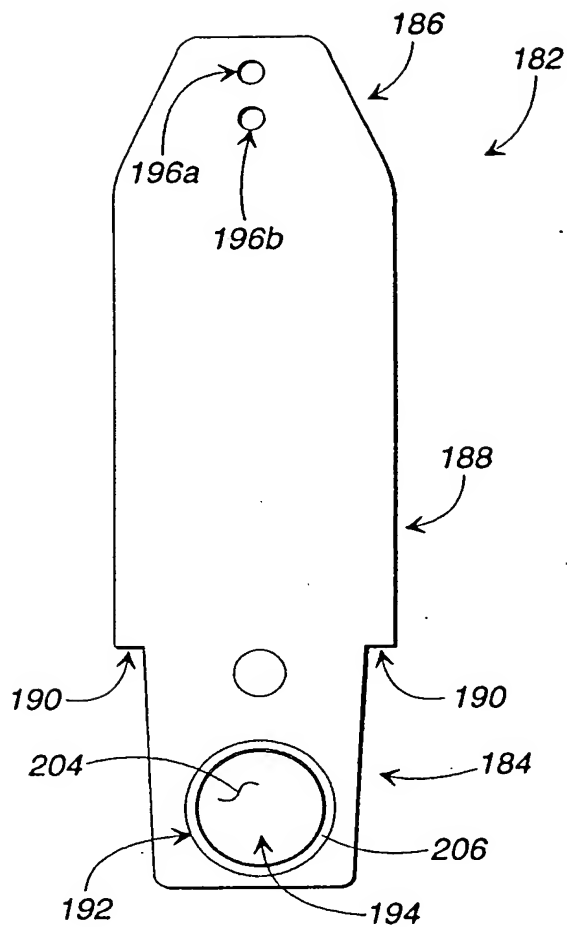


FIG. 12

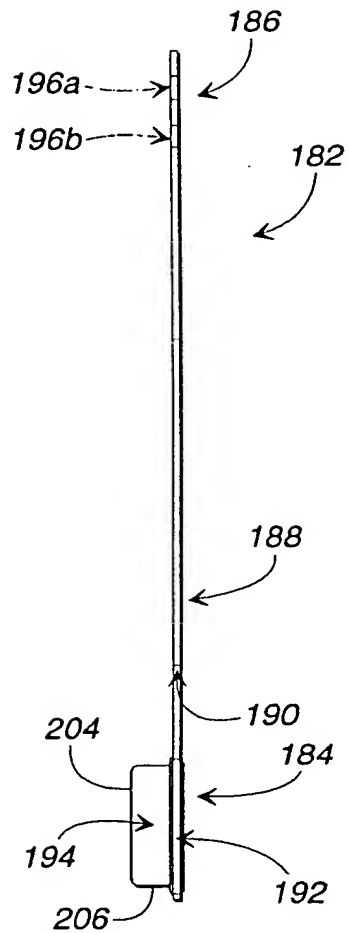


FIG. 13

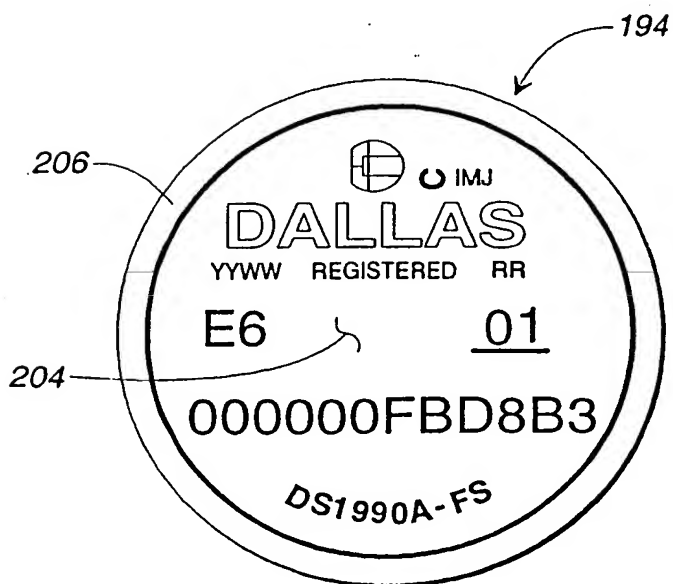


FIG. 14

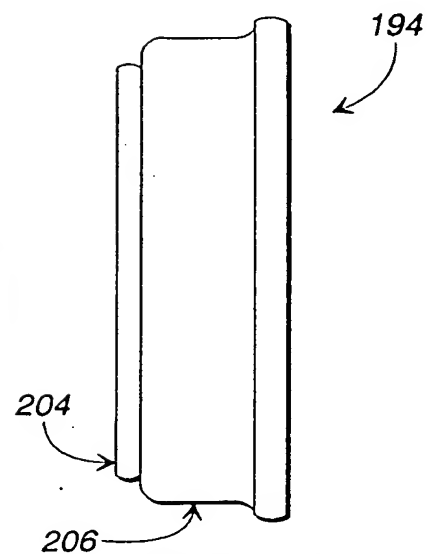


FIG. 15

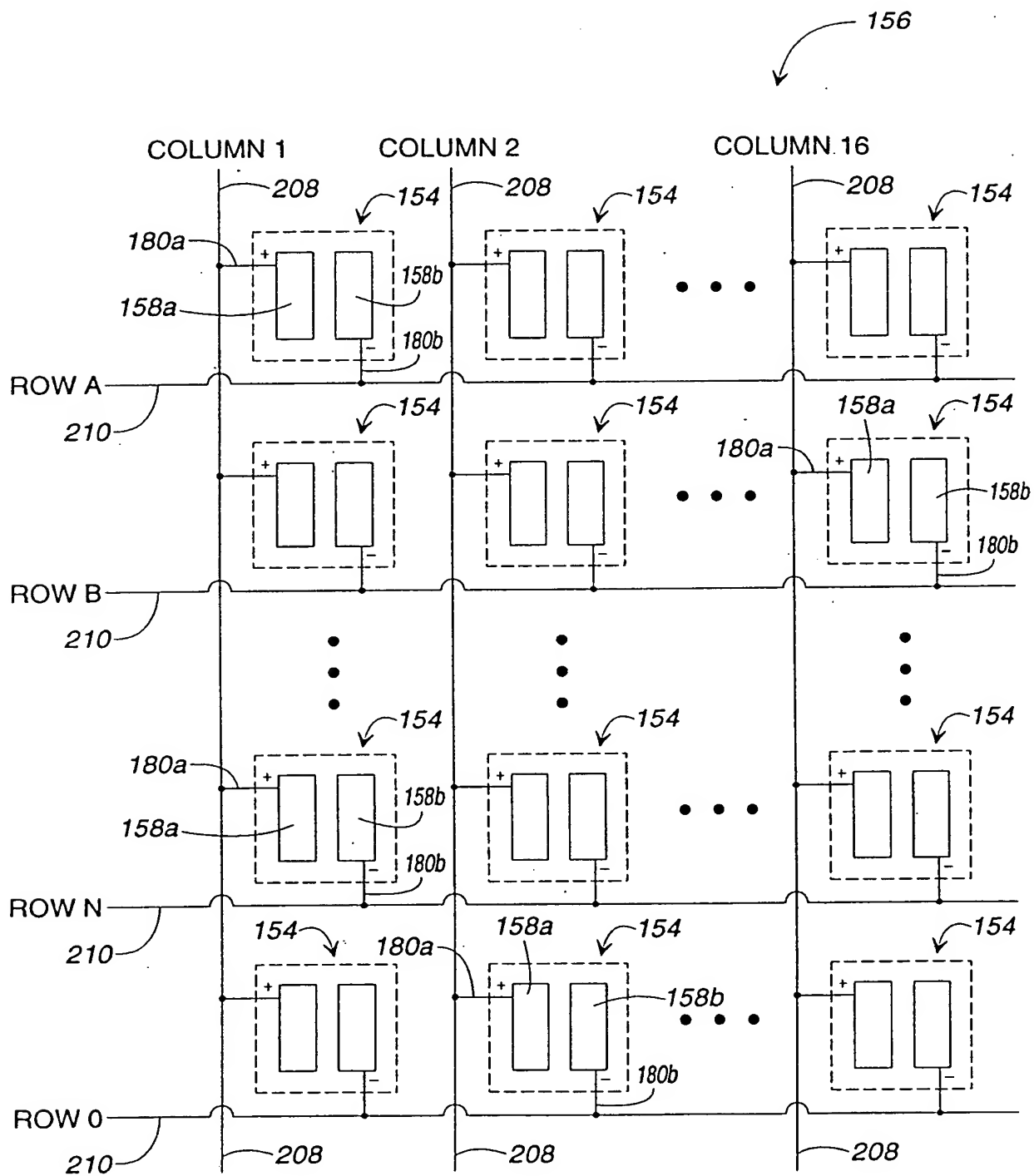


FIG. 16

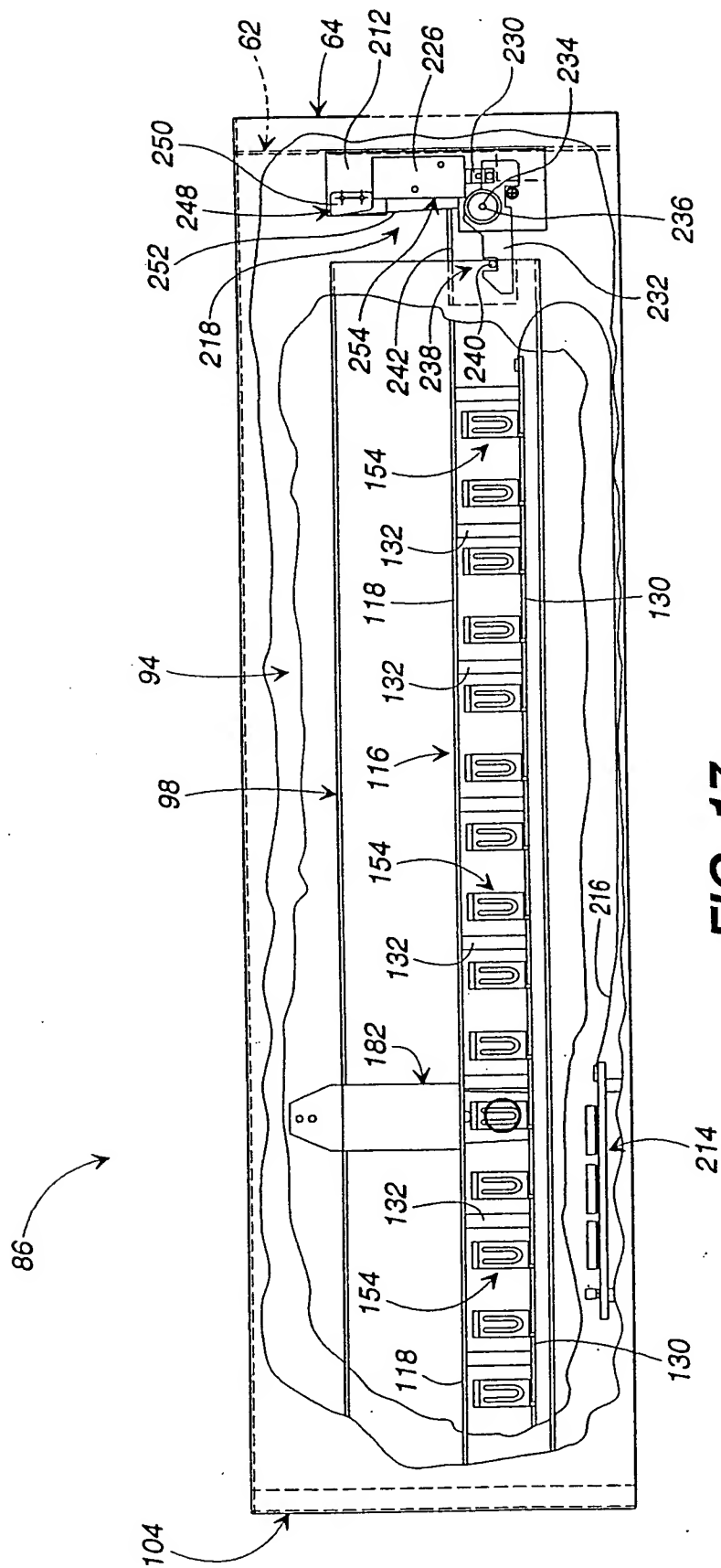
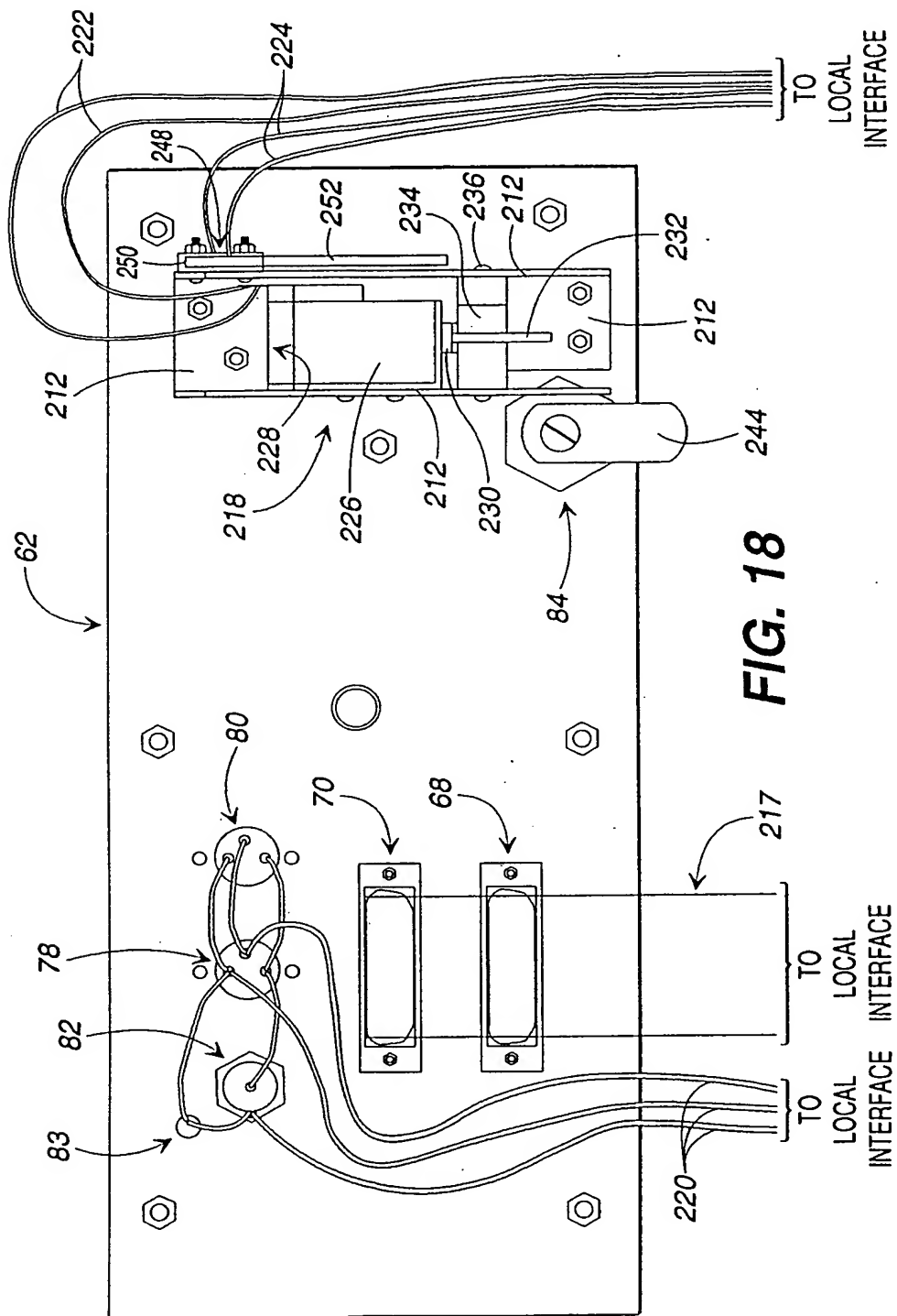


FIG. 17



The schematic diagram illustrates the power supply and enable logic for the 68000 microprocessor. It is divided into three main functional blocks by dashed lines: the **POWER SUPPLY** block, the **ENABLE DW** (Data Word) block, and the **68000** microprocessor block.

POWER SUPPLY: This block contains a 5V regulator circuit. It features a 7805 voltage regulator IC, a 0.1μF capacitor at the input, and a 0.1μF capacitor at the output. The output of the regulator is connected to the VCC pin of the 68000 microprocessor. A 100kΩ resistor is connected between the VCC pin and the GND pin to ensure proper initialization.

ENABLE DW: This block contains the logic for enabling the data word bus. It includes an AND gate with two inputs: one connected to the \overline{OE} (active-low output enable) pin of the 68000 microprocessor, and the other connected to a 5V supply. The output of the AND gate is connected to the \overline{EN} (active-low enable) pin of the 68000 microprocessor. A 100kΩ resistor is connected between the \overline{EN} pin and the 5V supply to ensure it is pulled up when not active.

68000: The 68000 microprocessor is shown with its pins connected to the power supply and enable logic. The VCC pin is connected to the 5V regulator output, and the GND pin is connected to ground. The \overline{OE} pin is connected to the AND gate input, and the \overline{EN} pin is connected to the AND gate output. The data bus pins (D0-D31) are connected to the data bus lines.

MATCH LINE TO FIG. 19C

316-

318-

FIG. 19A

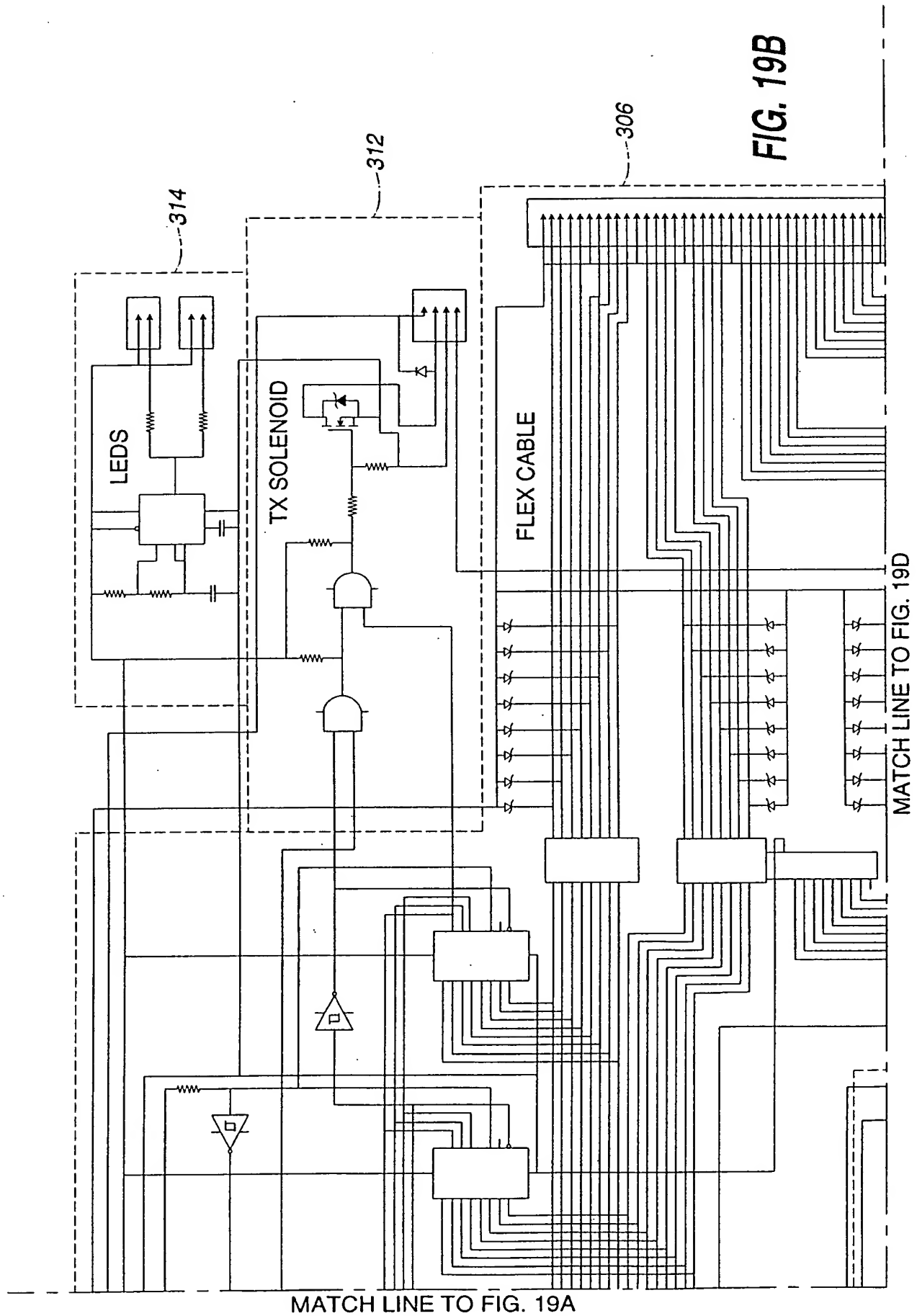


FIG. 19B

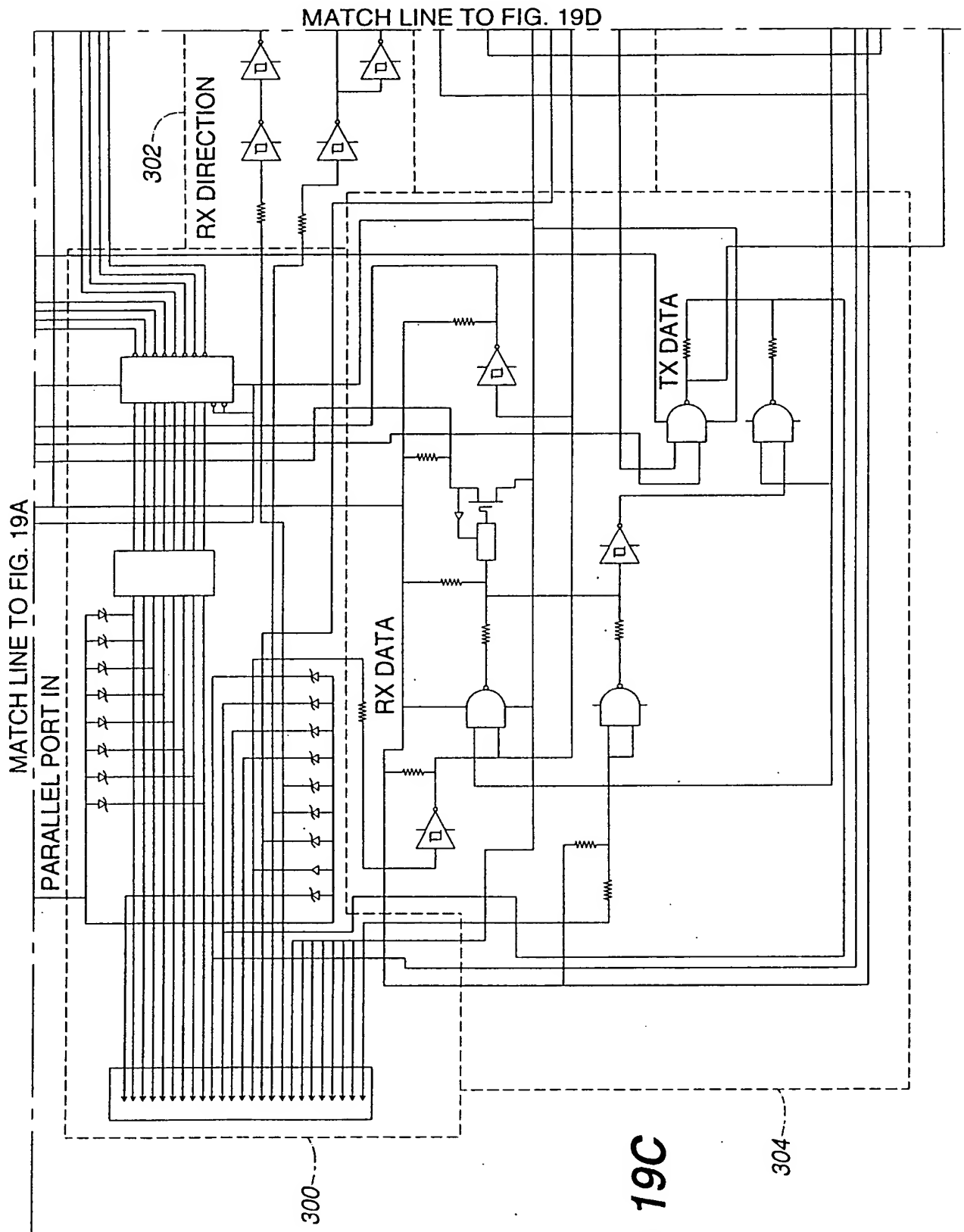
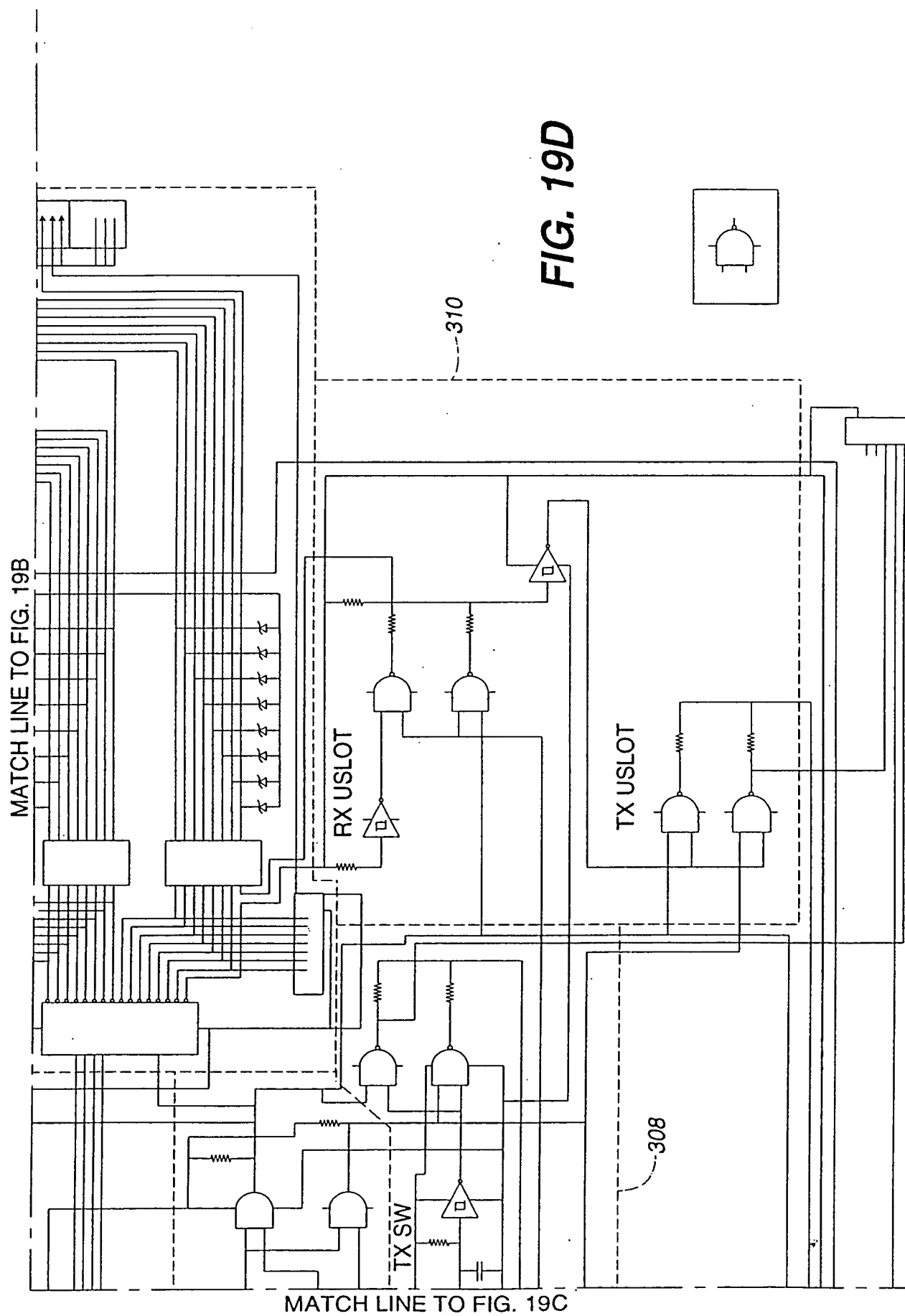


FIG. 19C



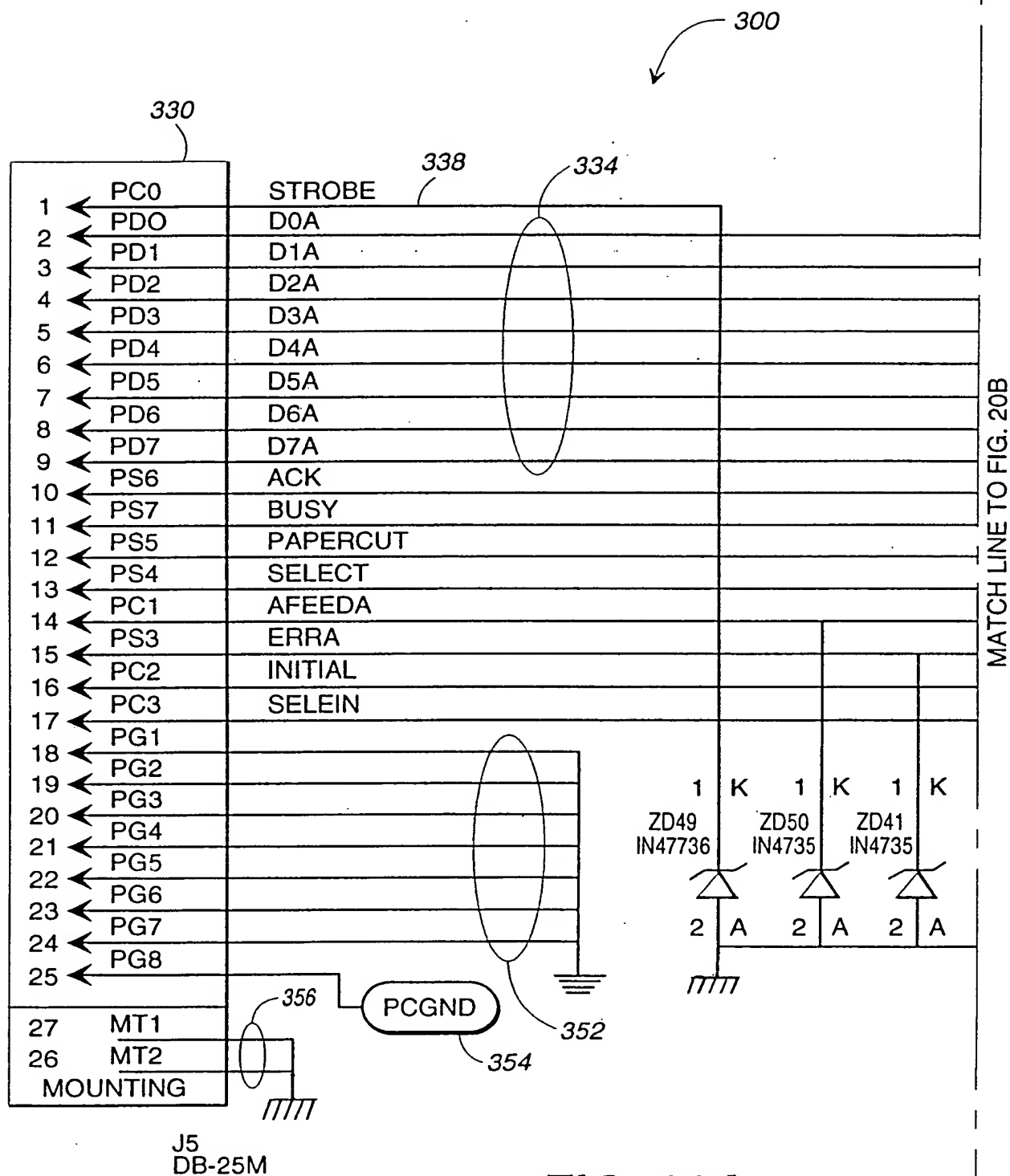
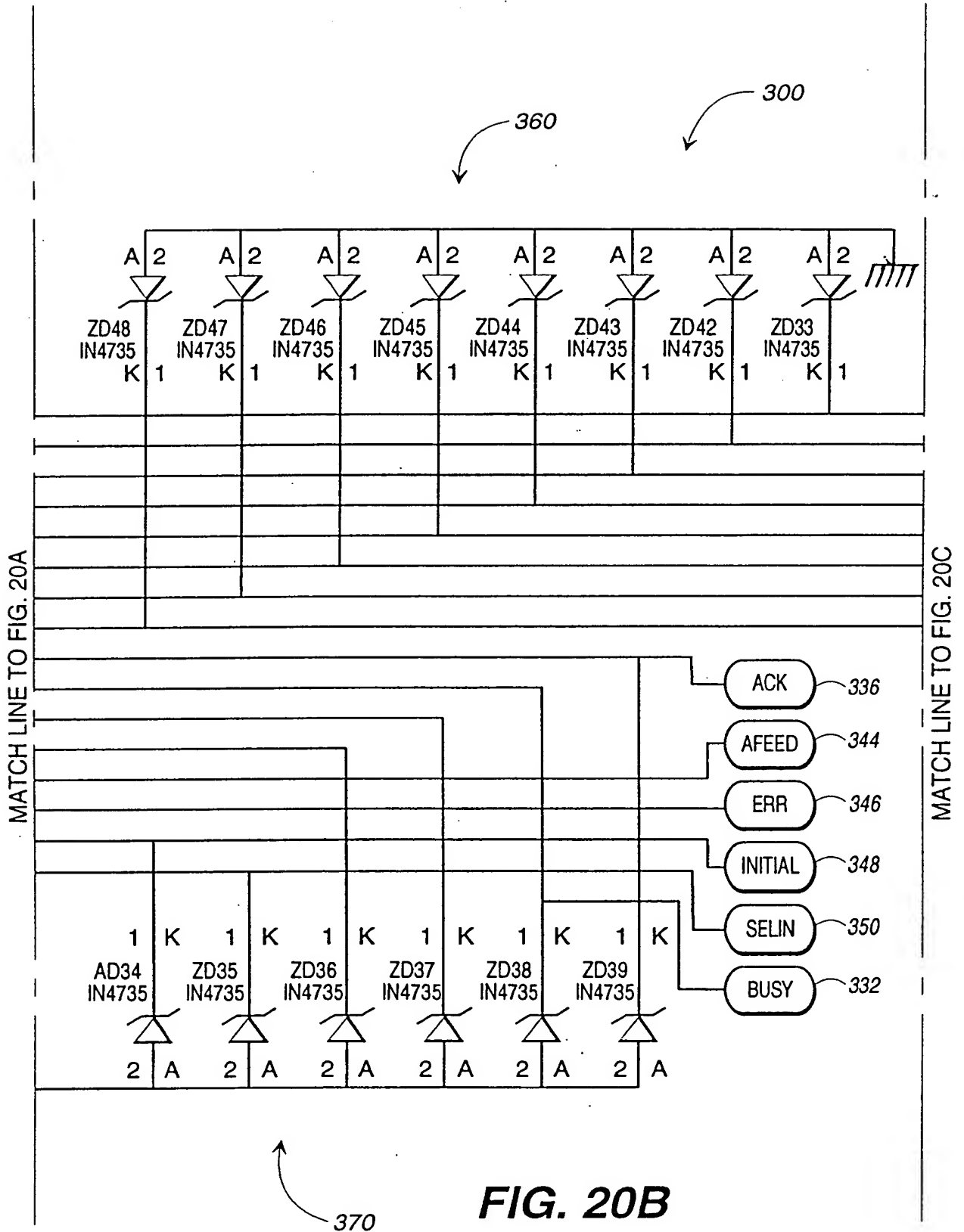


FIG. 20A



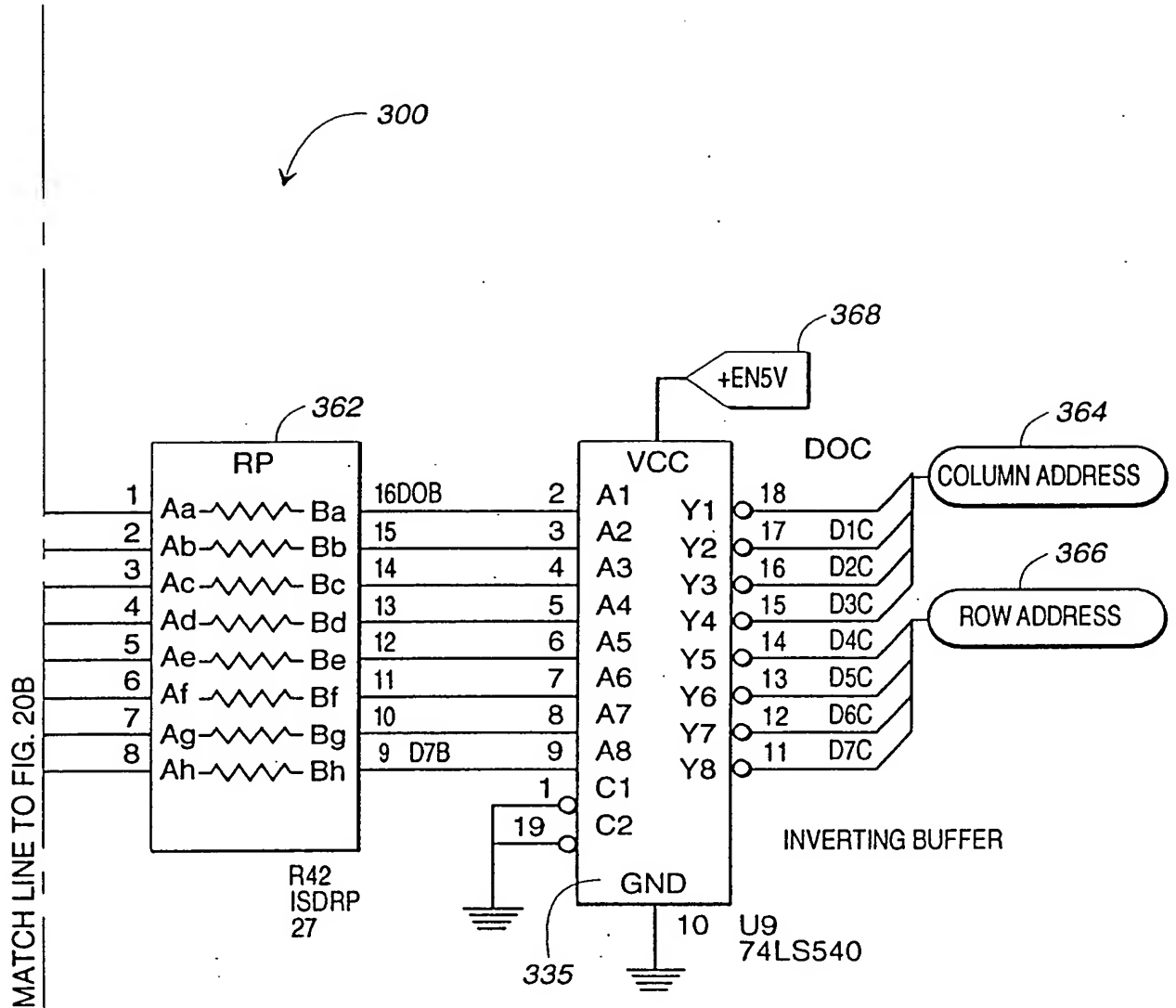
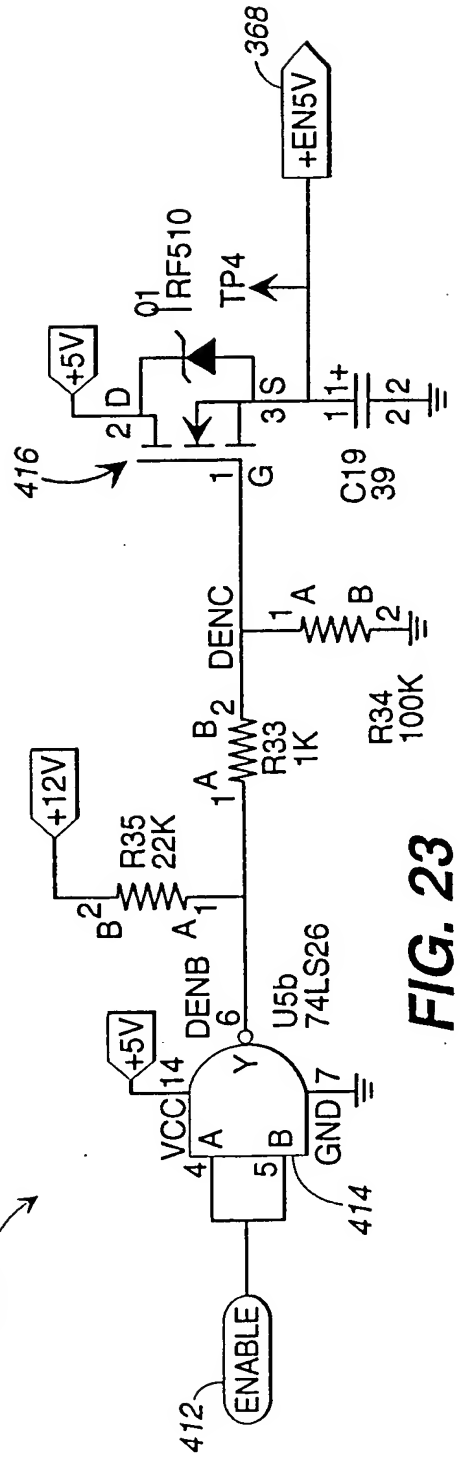
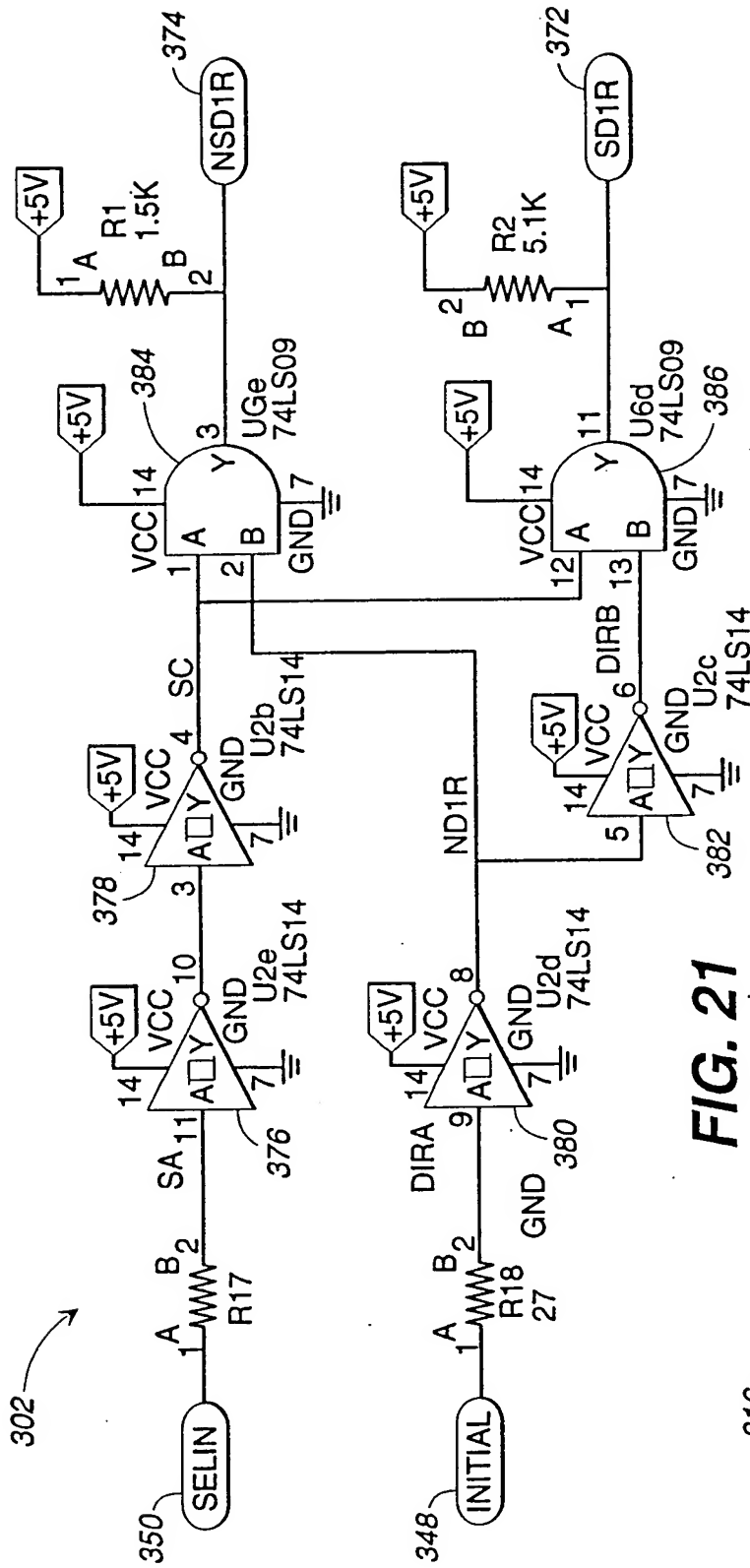


FIG. 20C



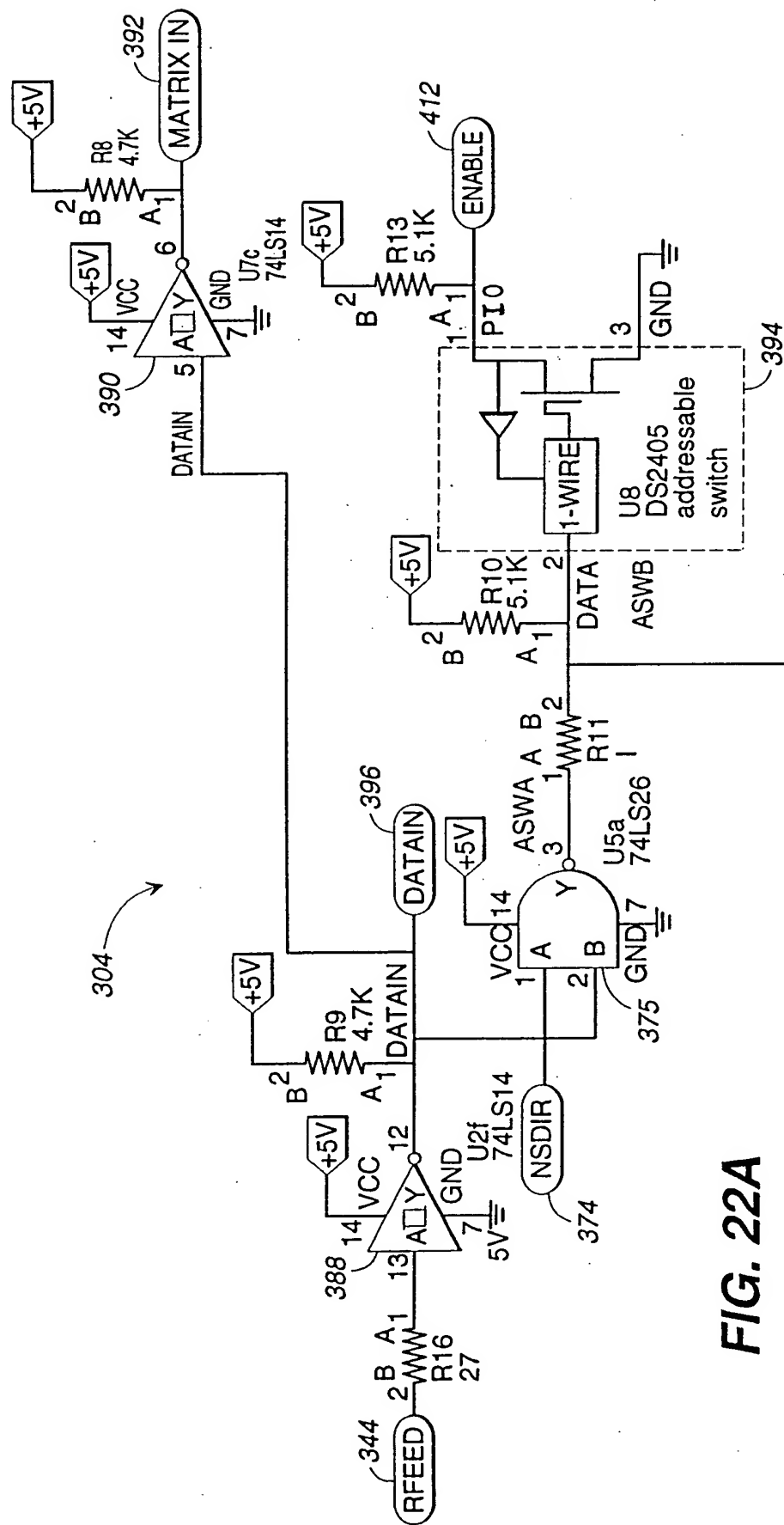


FIG. 22A

MATCH LINE TO FIG. 22B

306

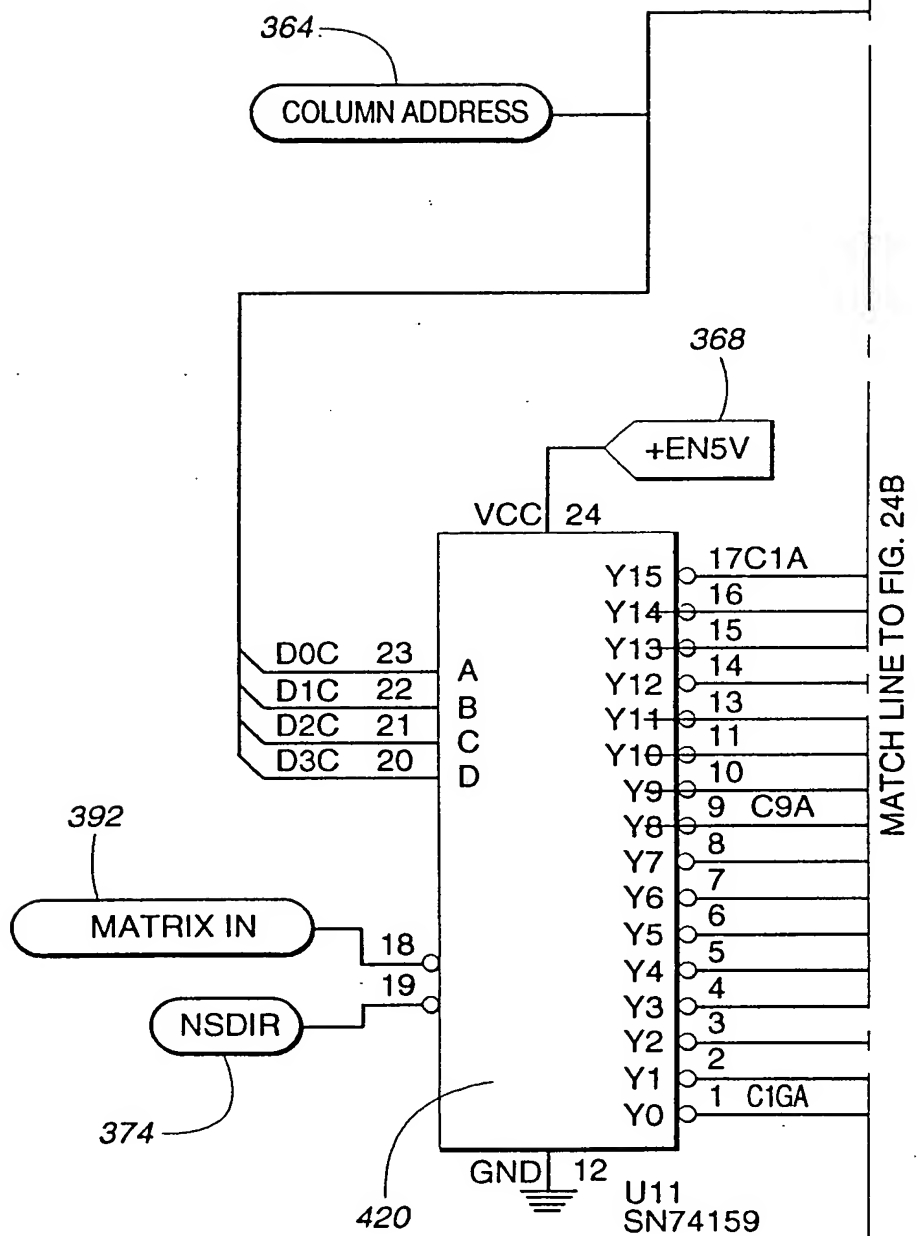
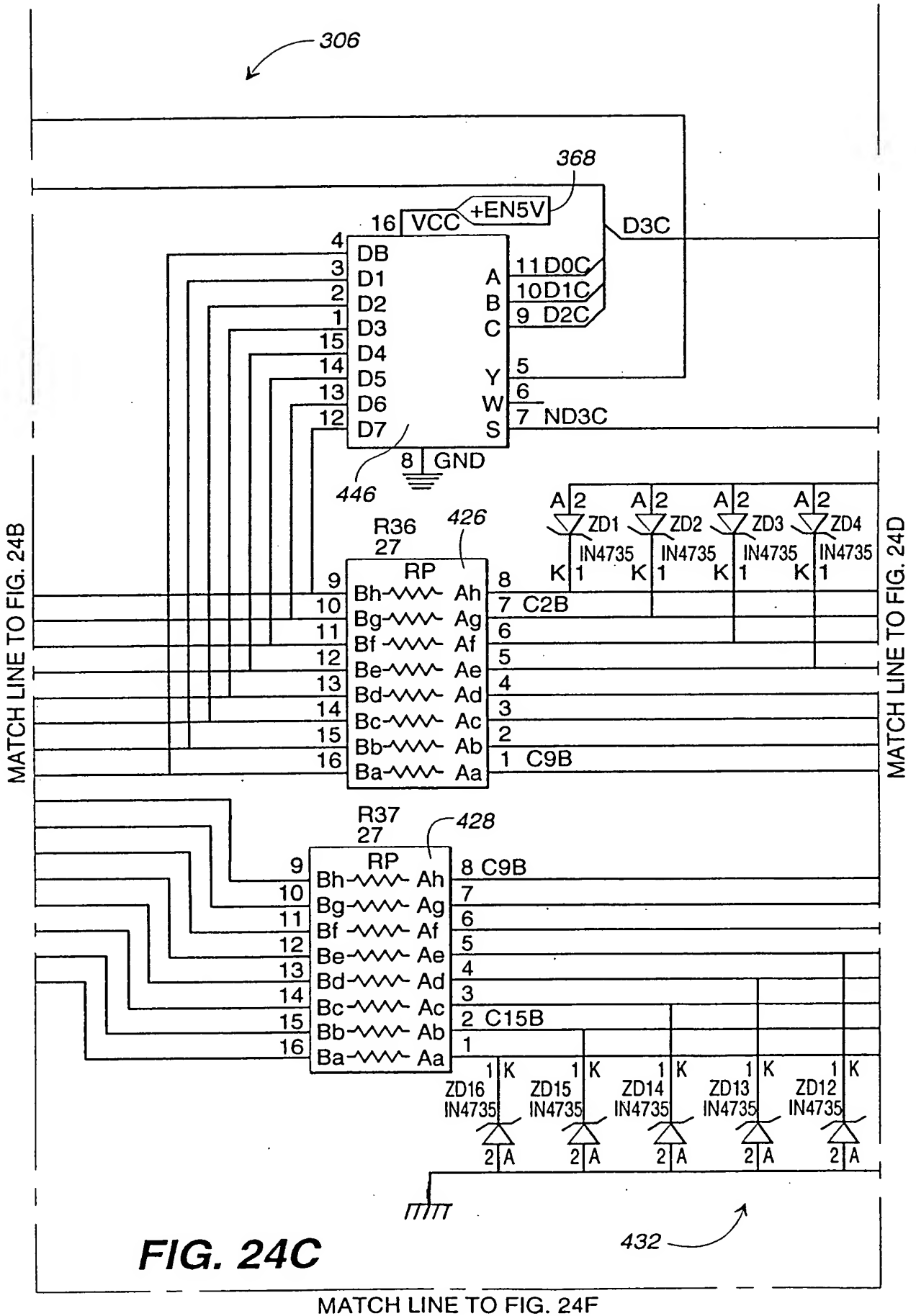


FIG. 24A



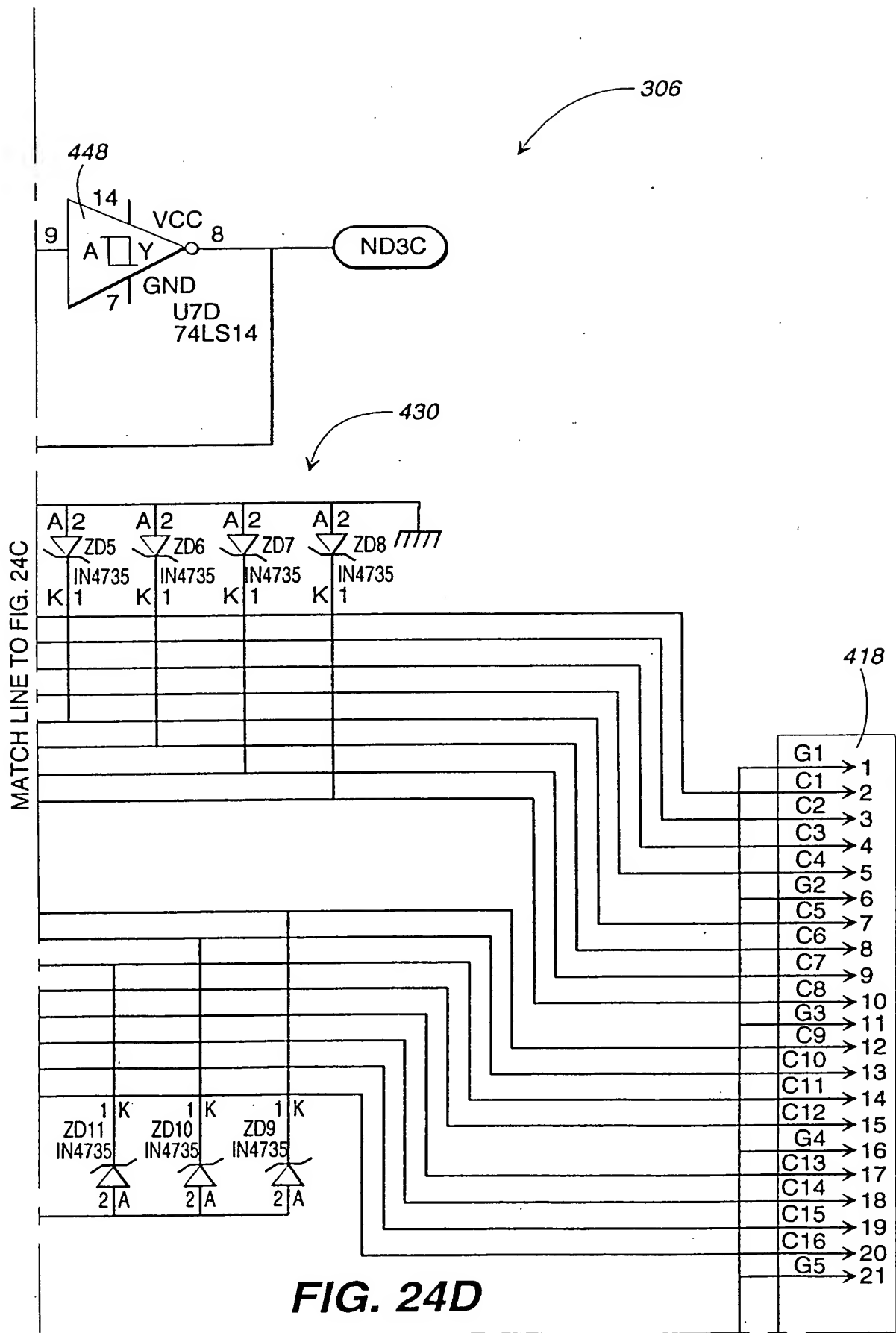
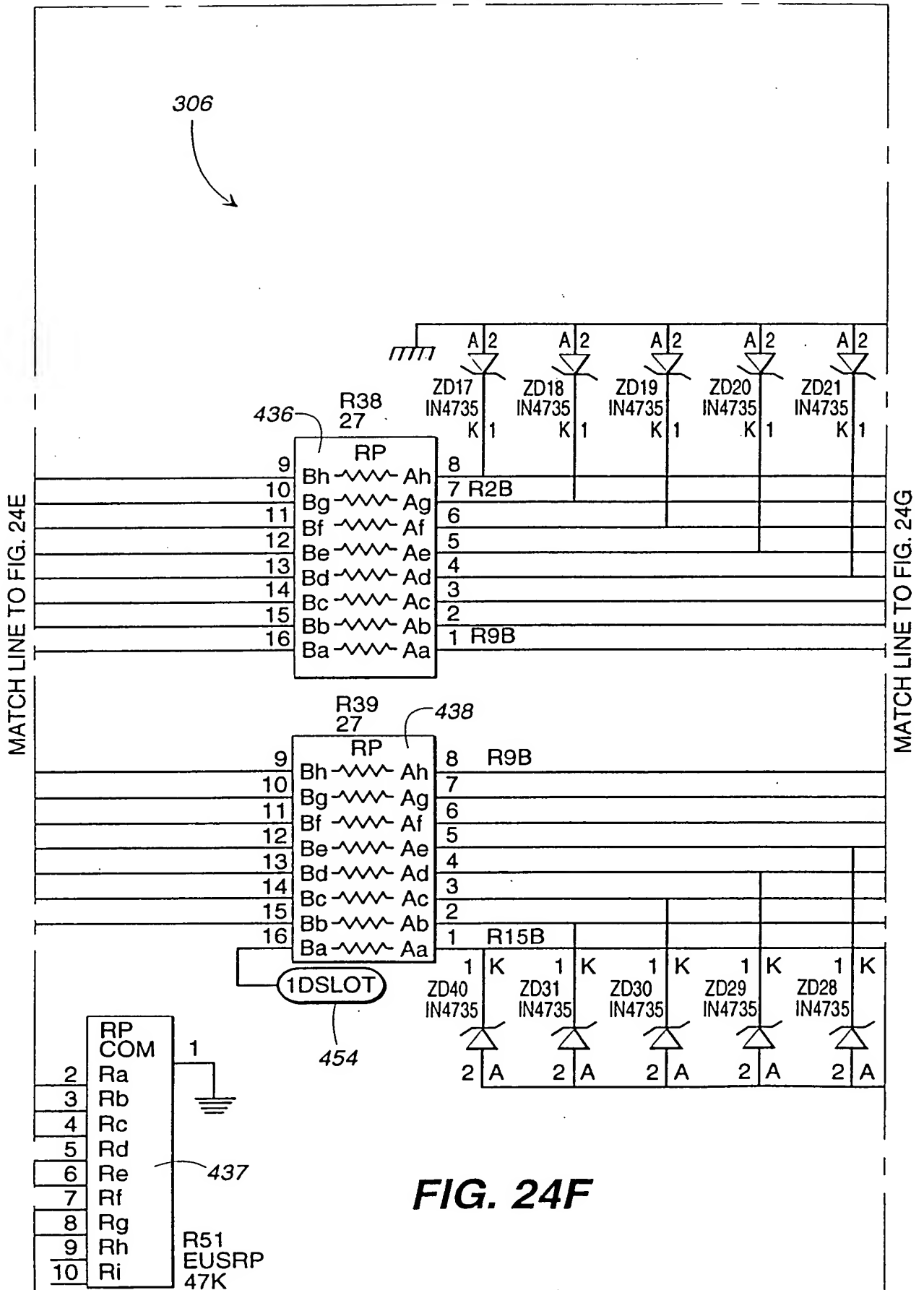


FIG. 24D

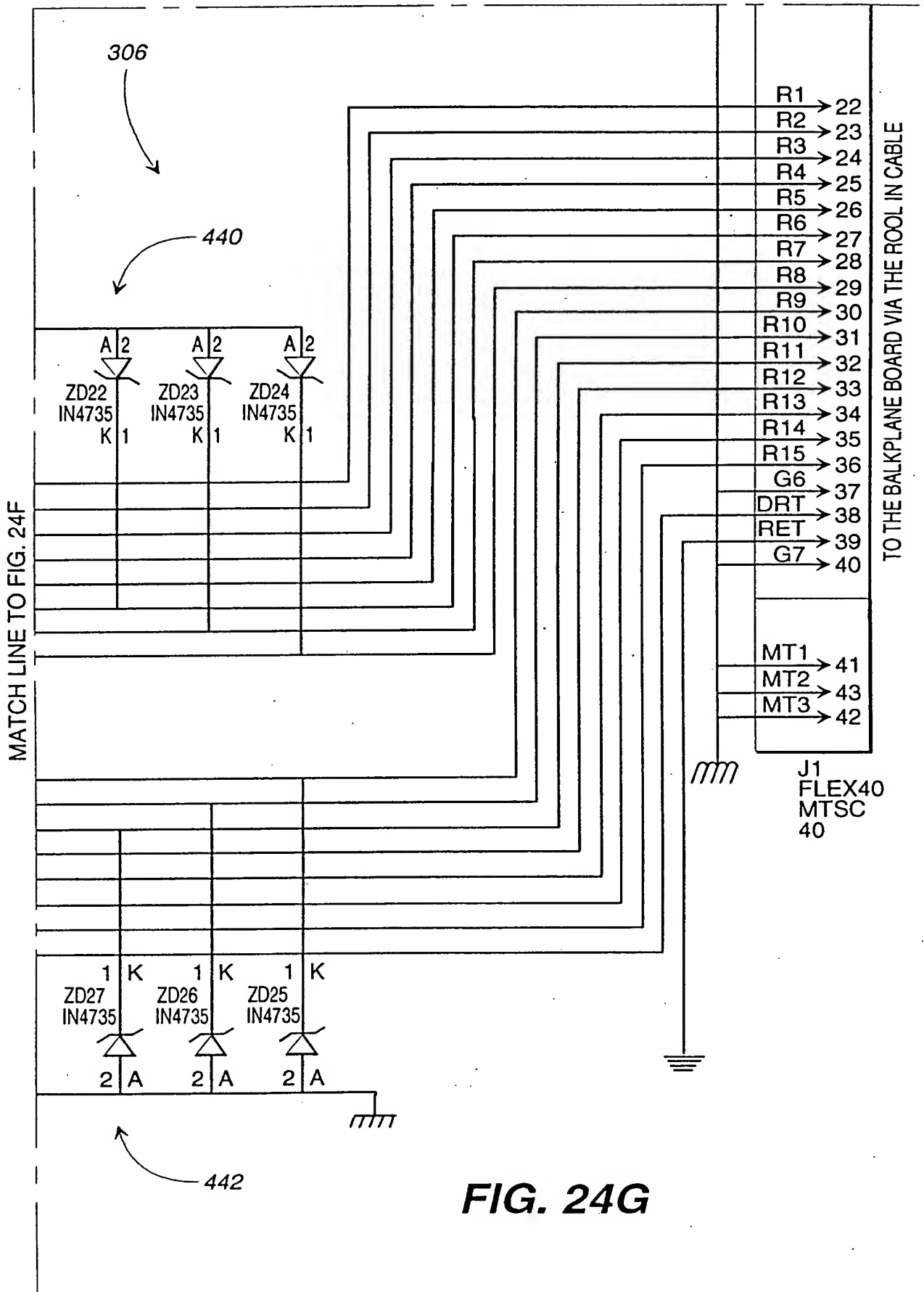
MATCH LINE TO FIG. 24G

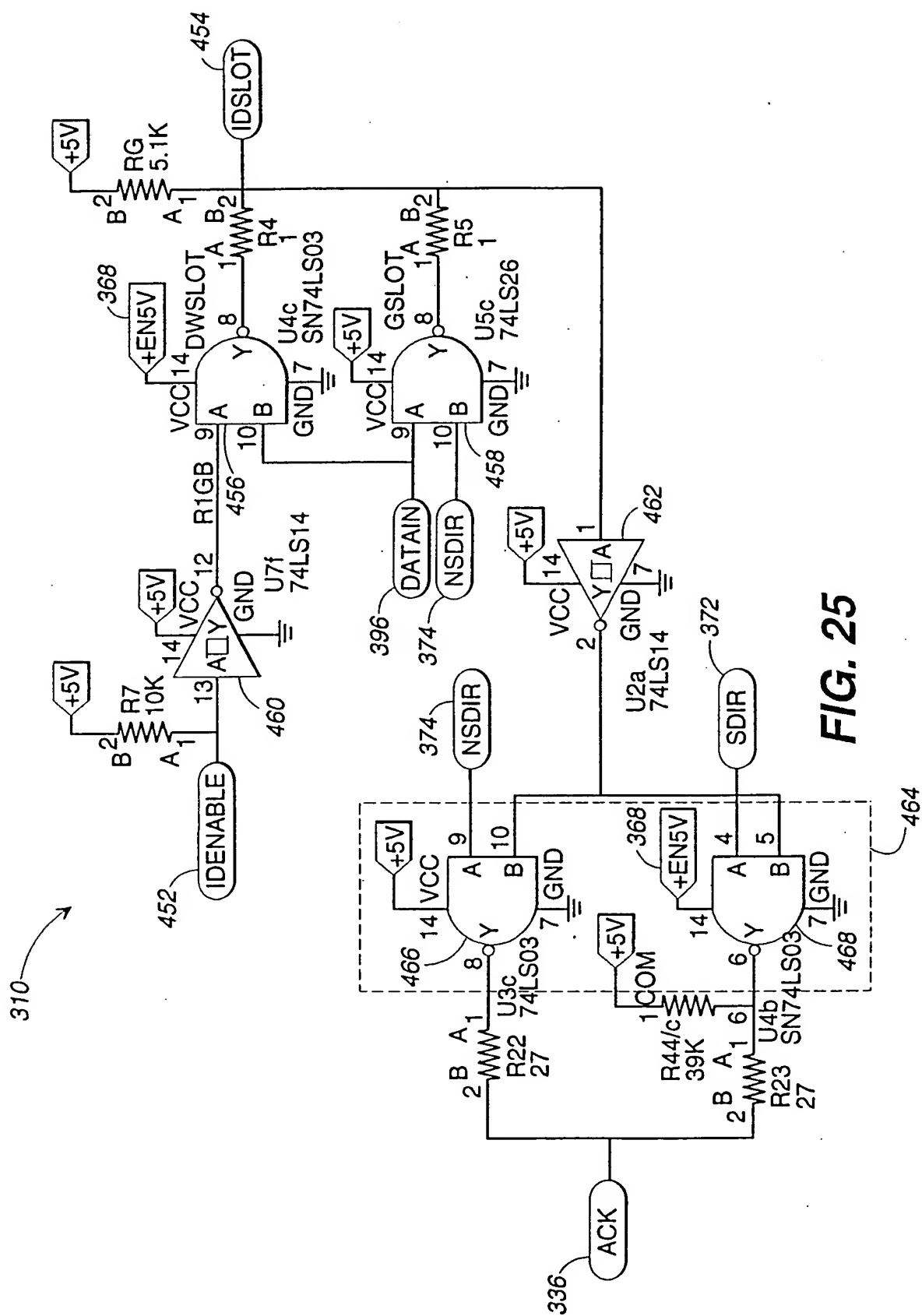


MATCH LINE TO FIG. 24C



MATCH LINE TO FIG. 24D





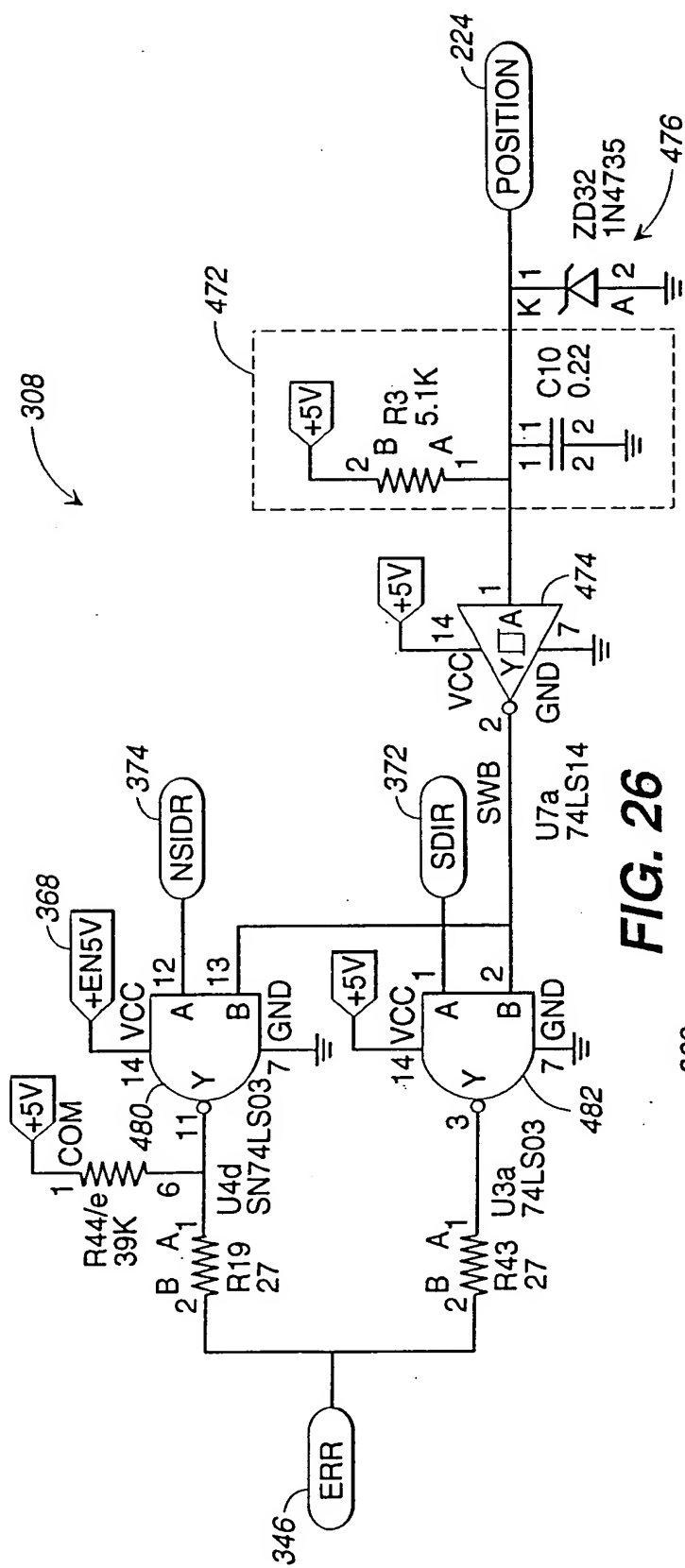


FIG. 26

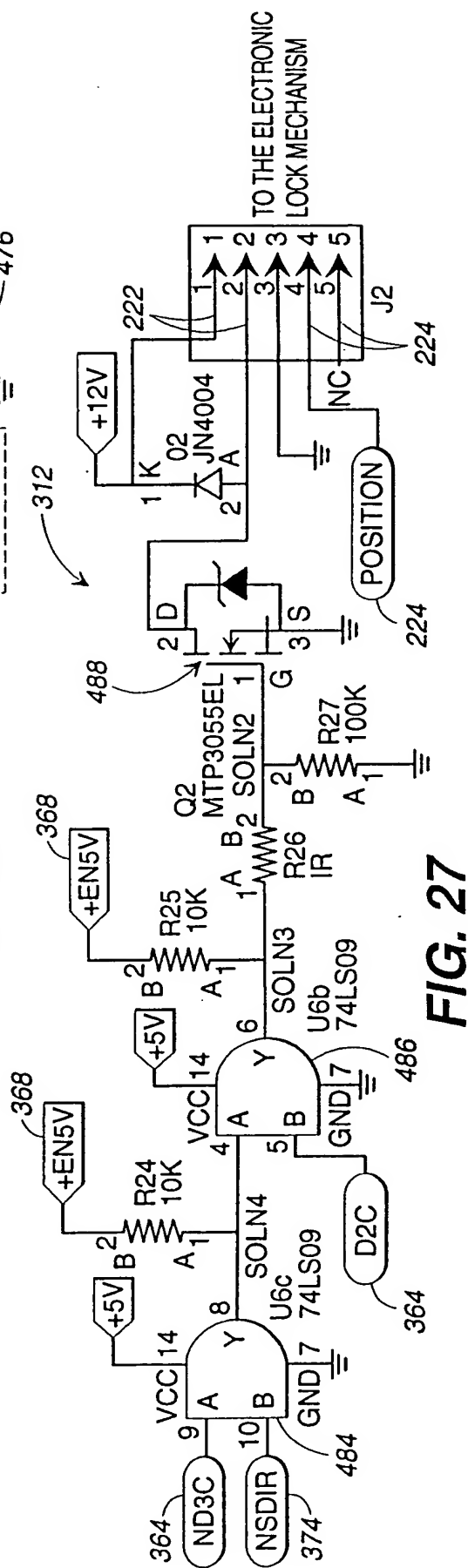


FIG. 27

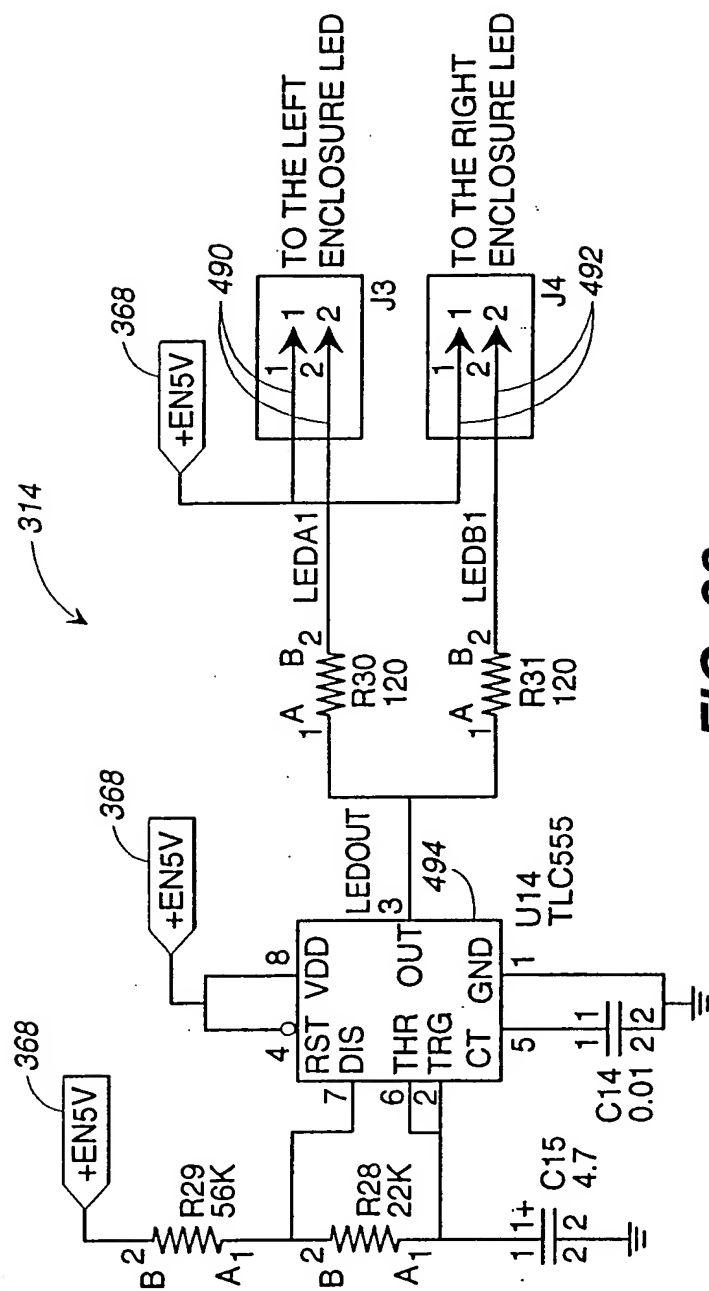


FIG. 28

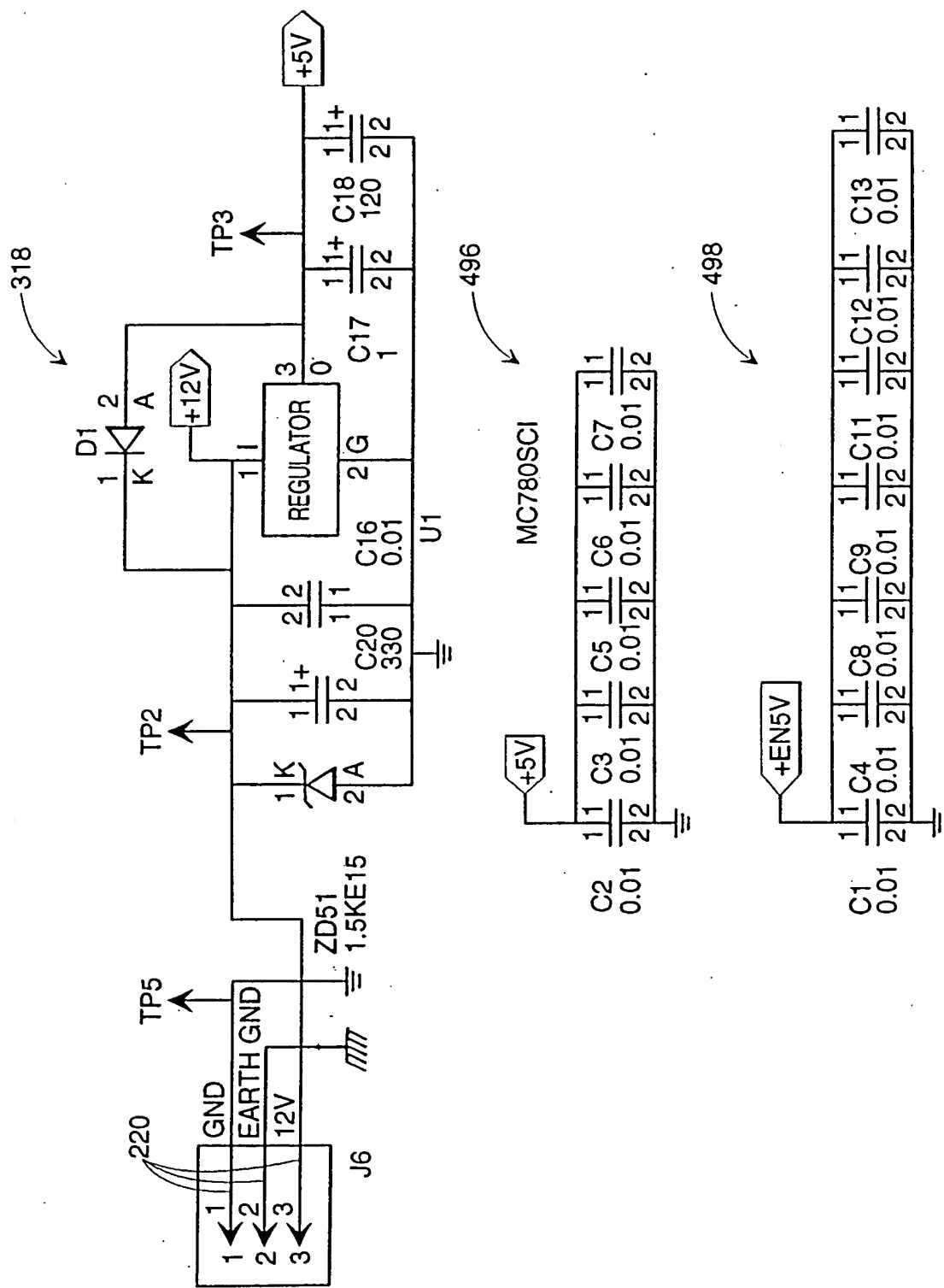
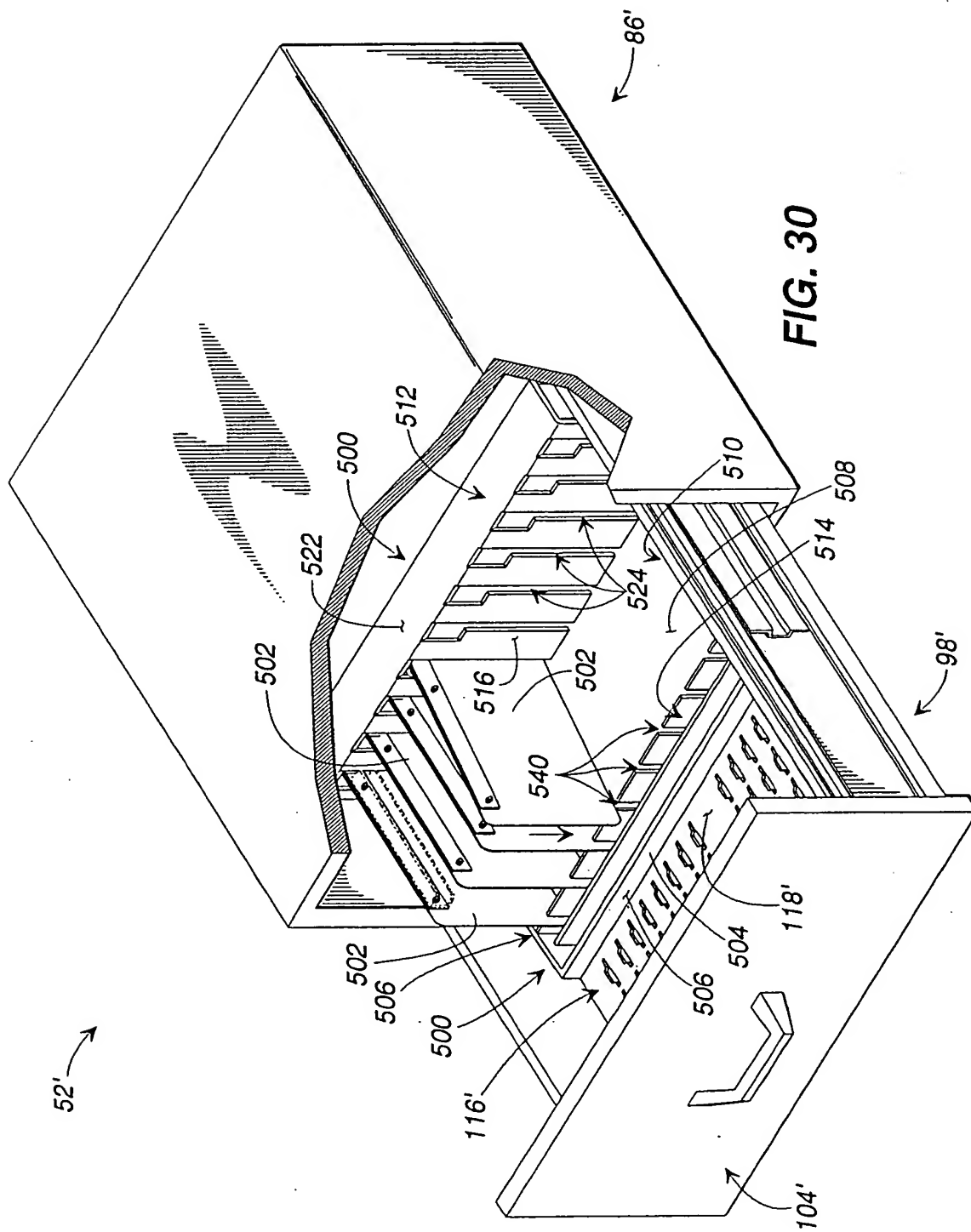


FIG. 29



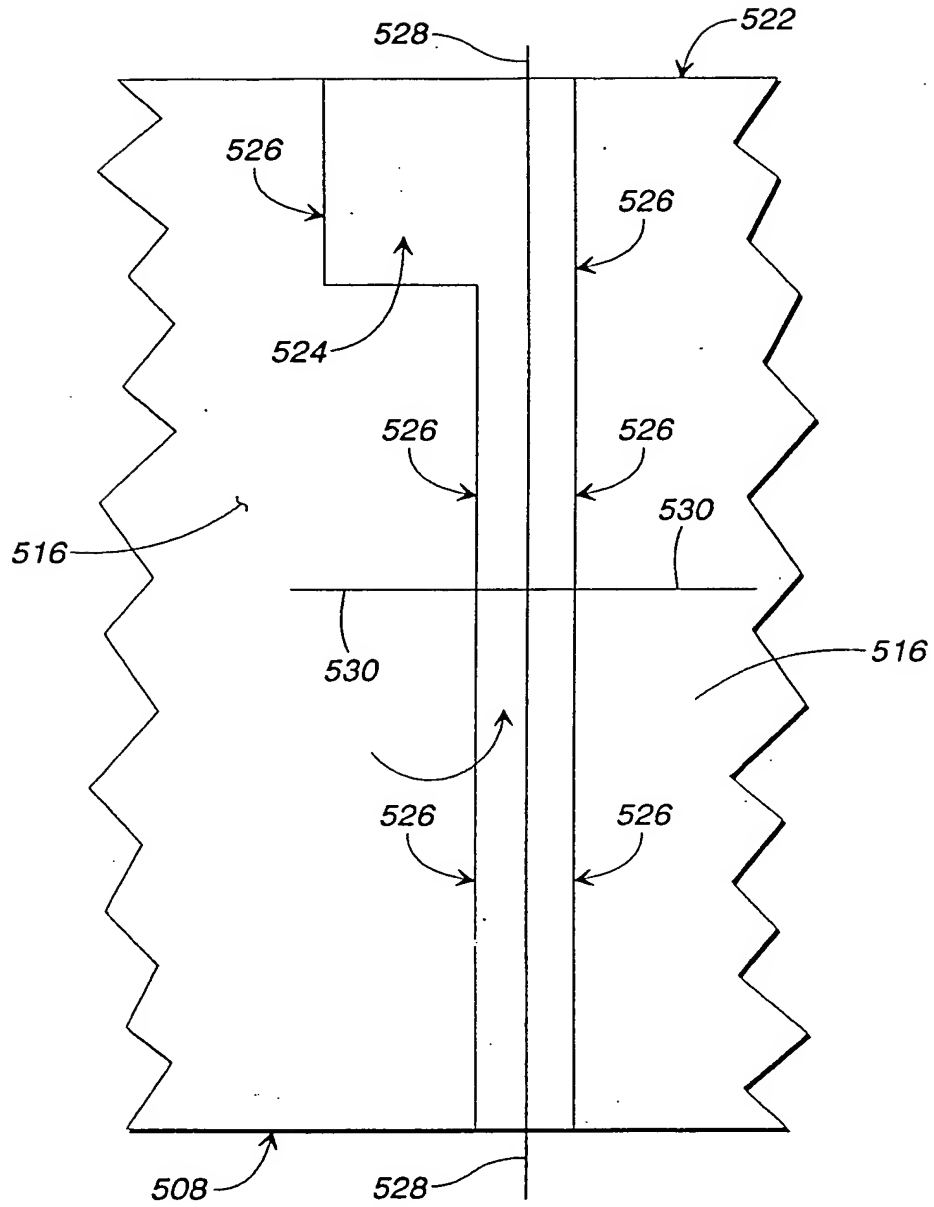


FIG. 31

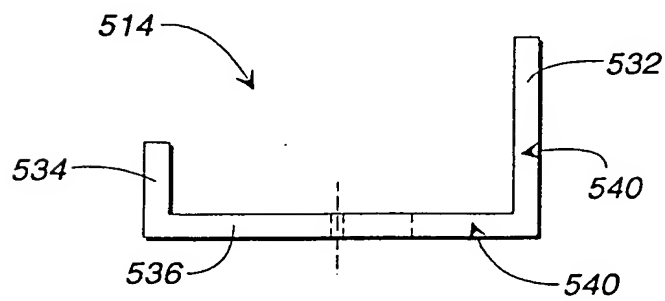


FIG. 32

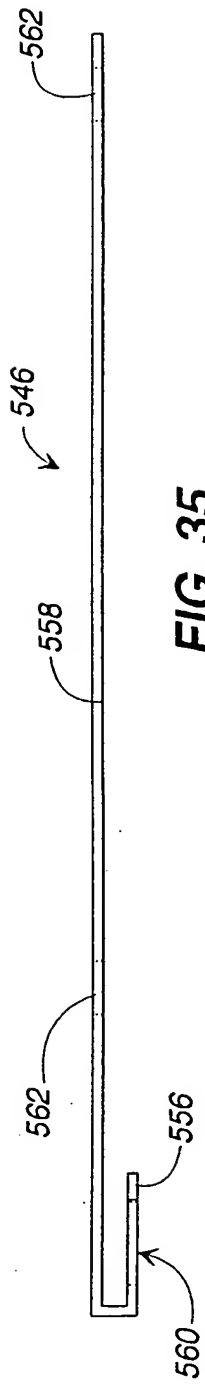


FIG. 35

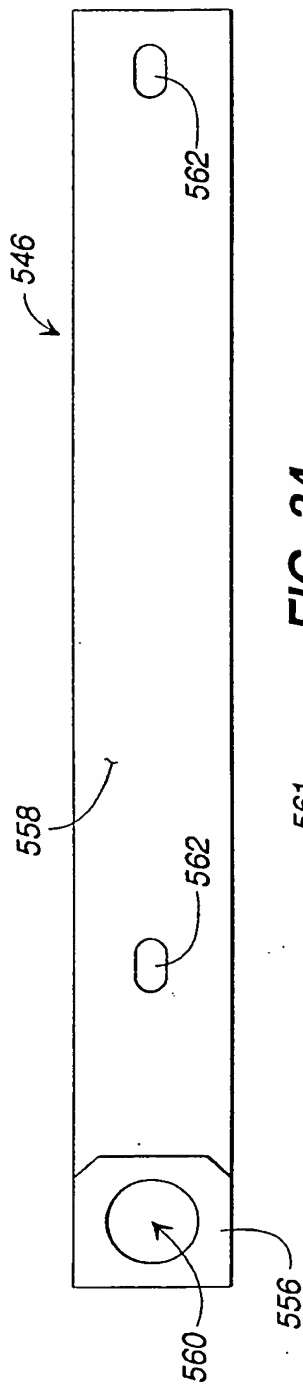


FIG. 34

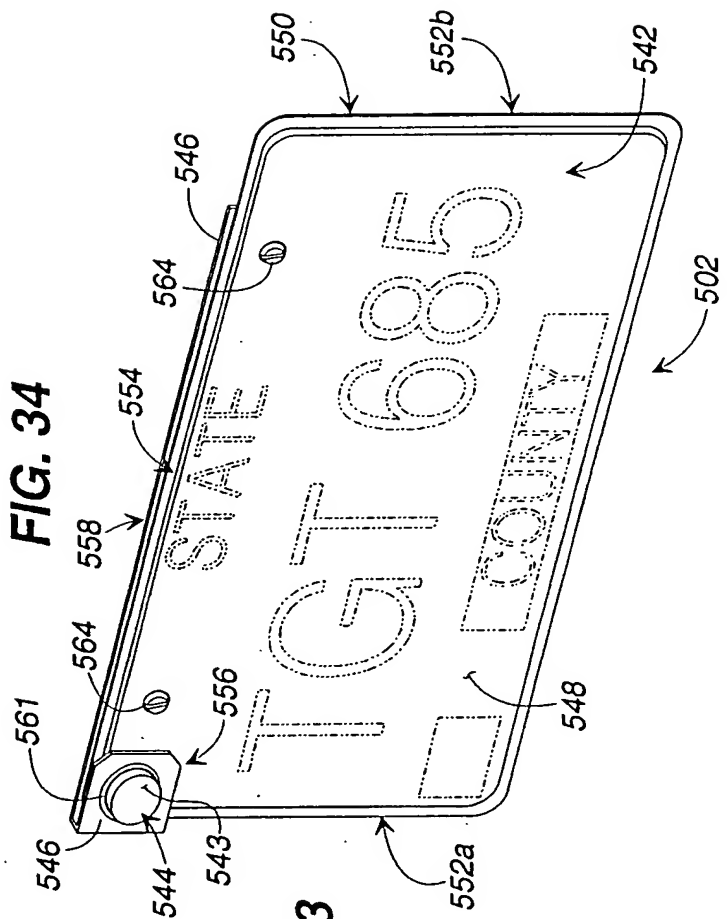
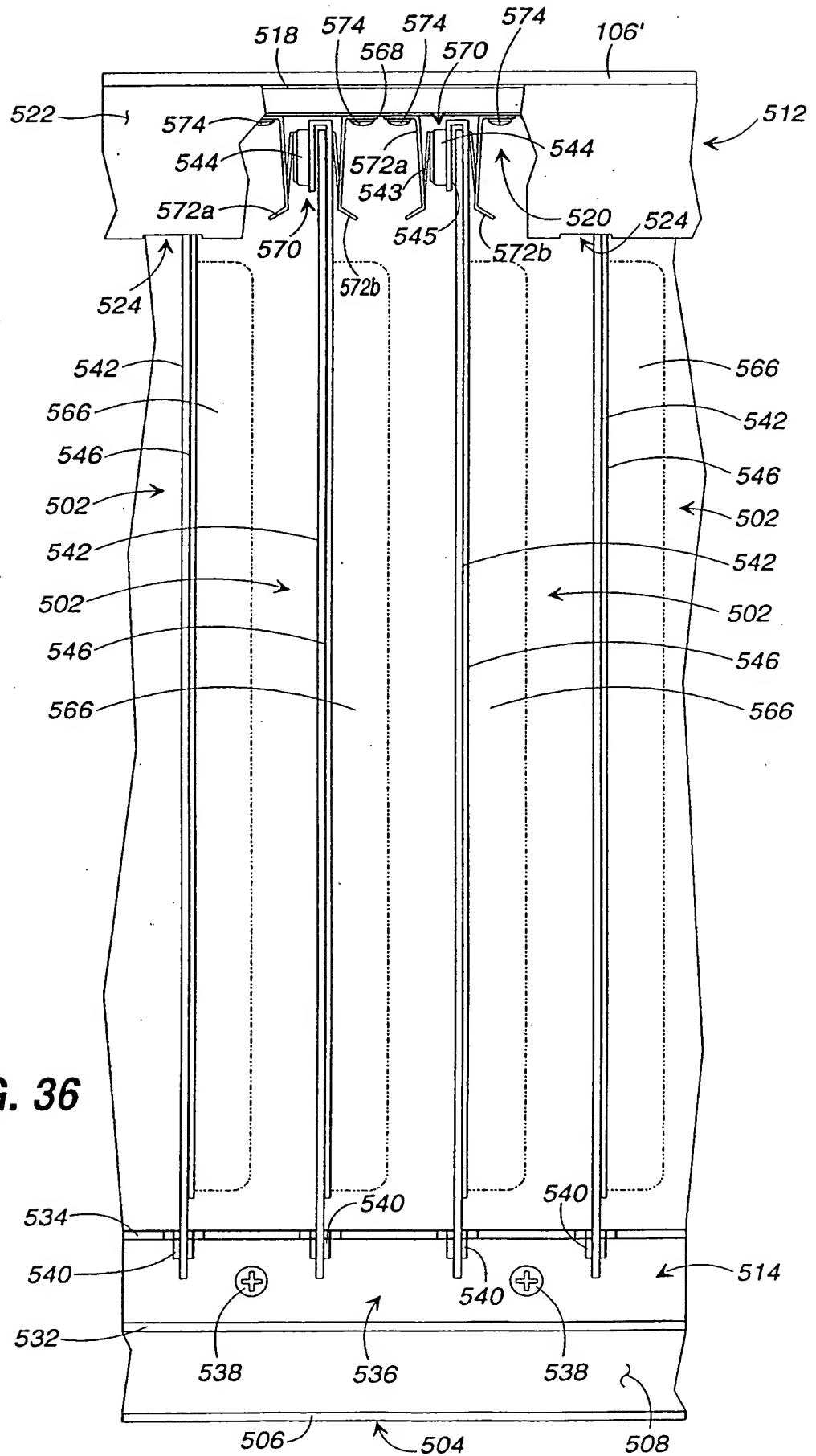


FIG. 33



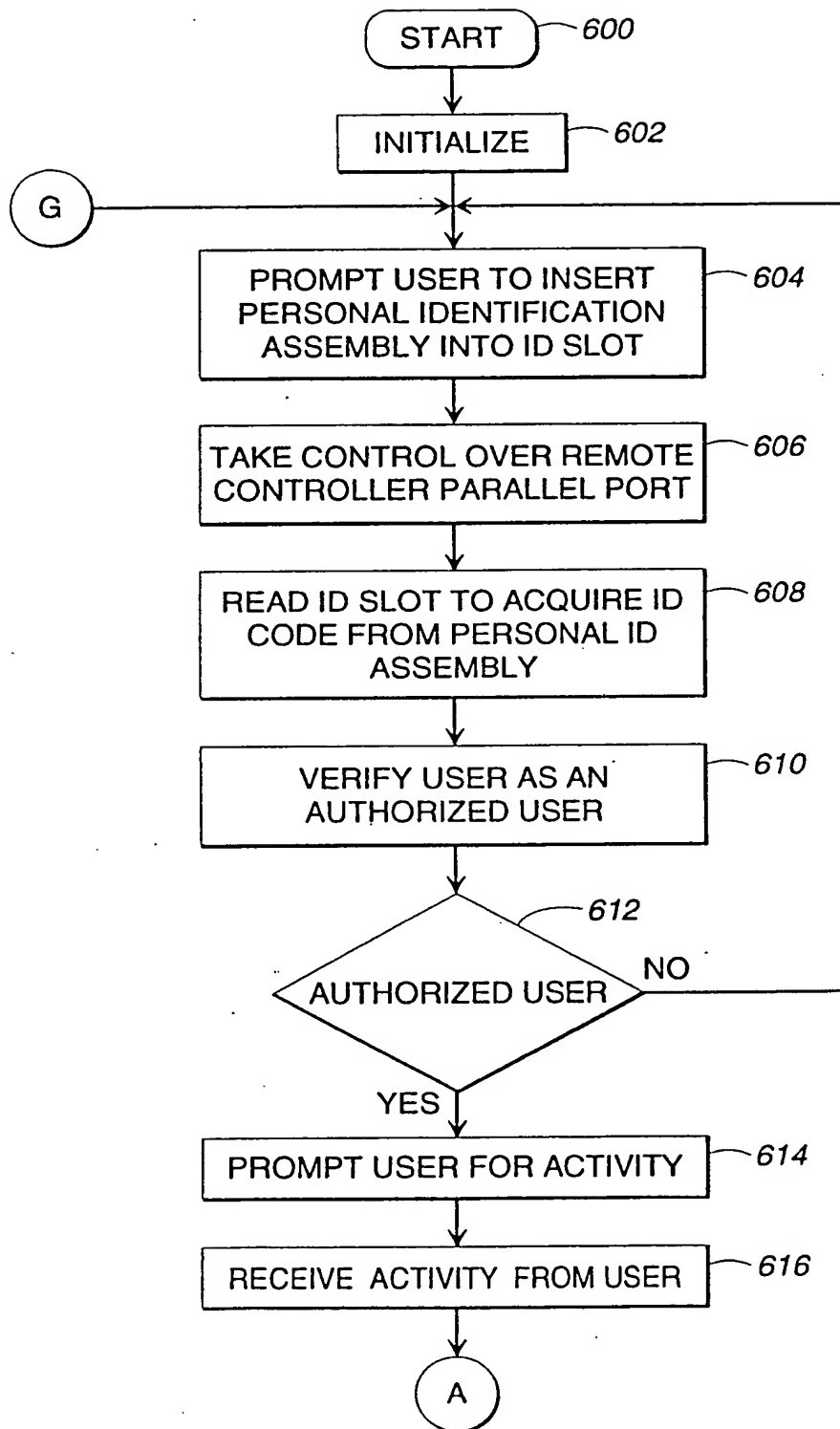


FIG. 37A

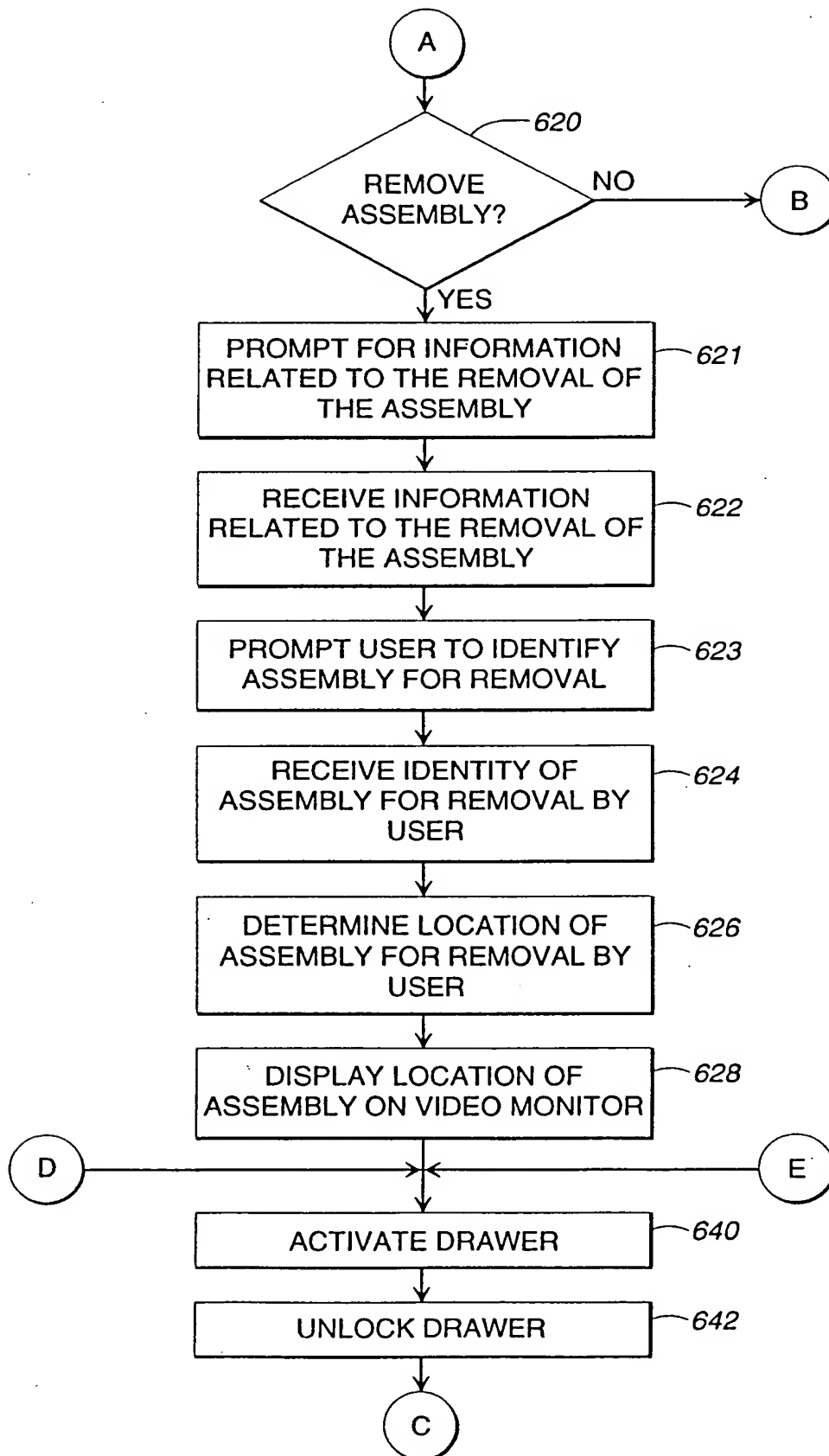


FIG. 37B

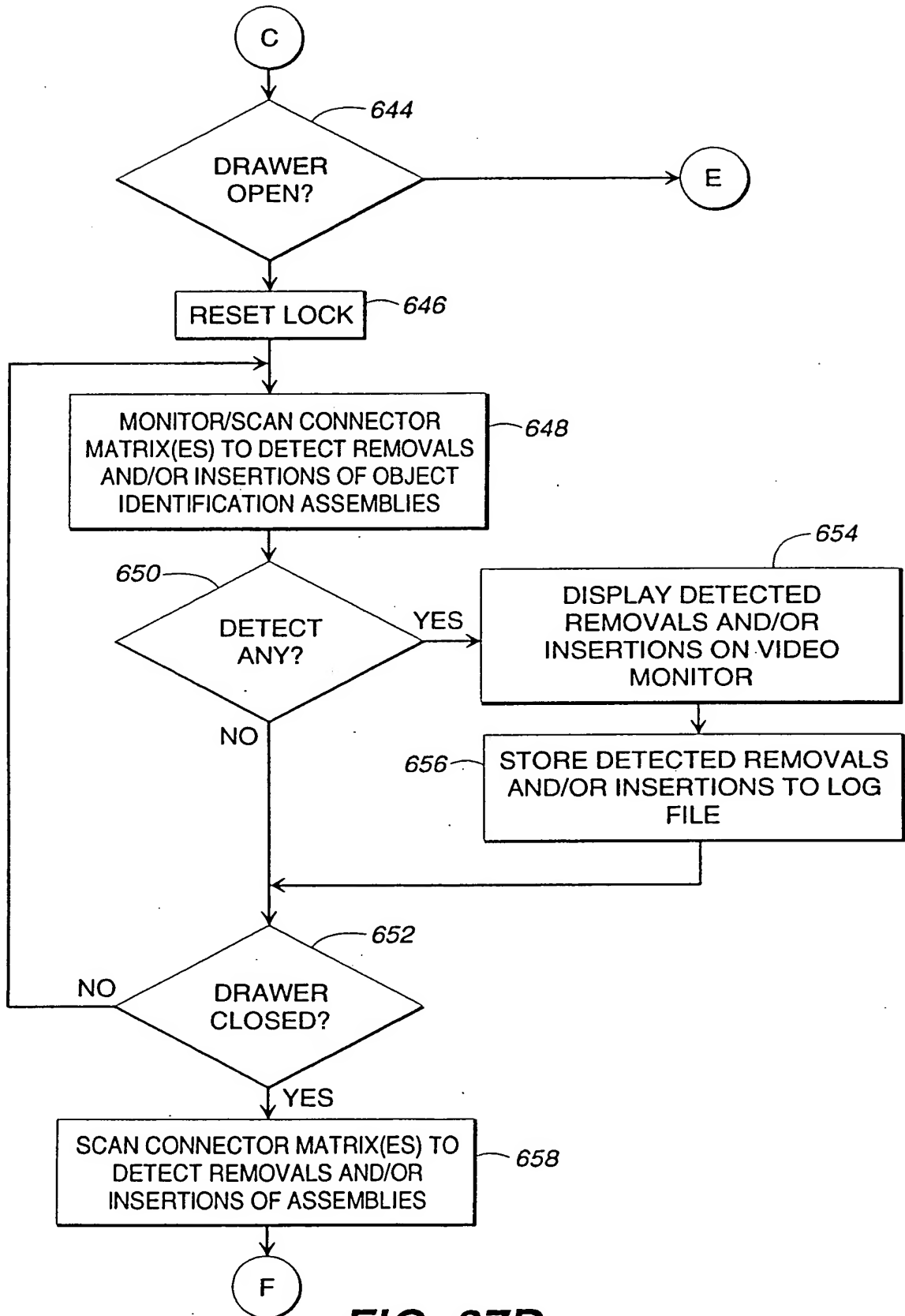


FIG. 37D

